

GA-MA790FX-DS5

Revision:1.0

SHEET TITLE

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02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
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05	AM2 DDR2 INTERFACE
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07	AM2 POWER
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09	DIMM 3,4
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11	RD790 HT & GFX I/F
12	RD790 GFX2 GPP SB I/F
13	RD790 CLOCK & SYSB I/F
14	RD790 POWER
15	RD790 STRAPS
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19	ATI SB600-SATA/IDE
20	ATI SB600-POWER
21	PCI Express x16-A
22	PCI Express x16-B
23	PCIE 1,2,3 , PCI SLOT 1,2
24	IDE/FDD
25	COMA,LPT,USB PORT

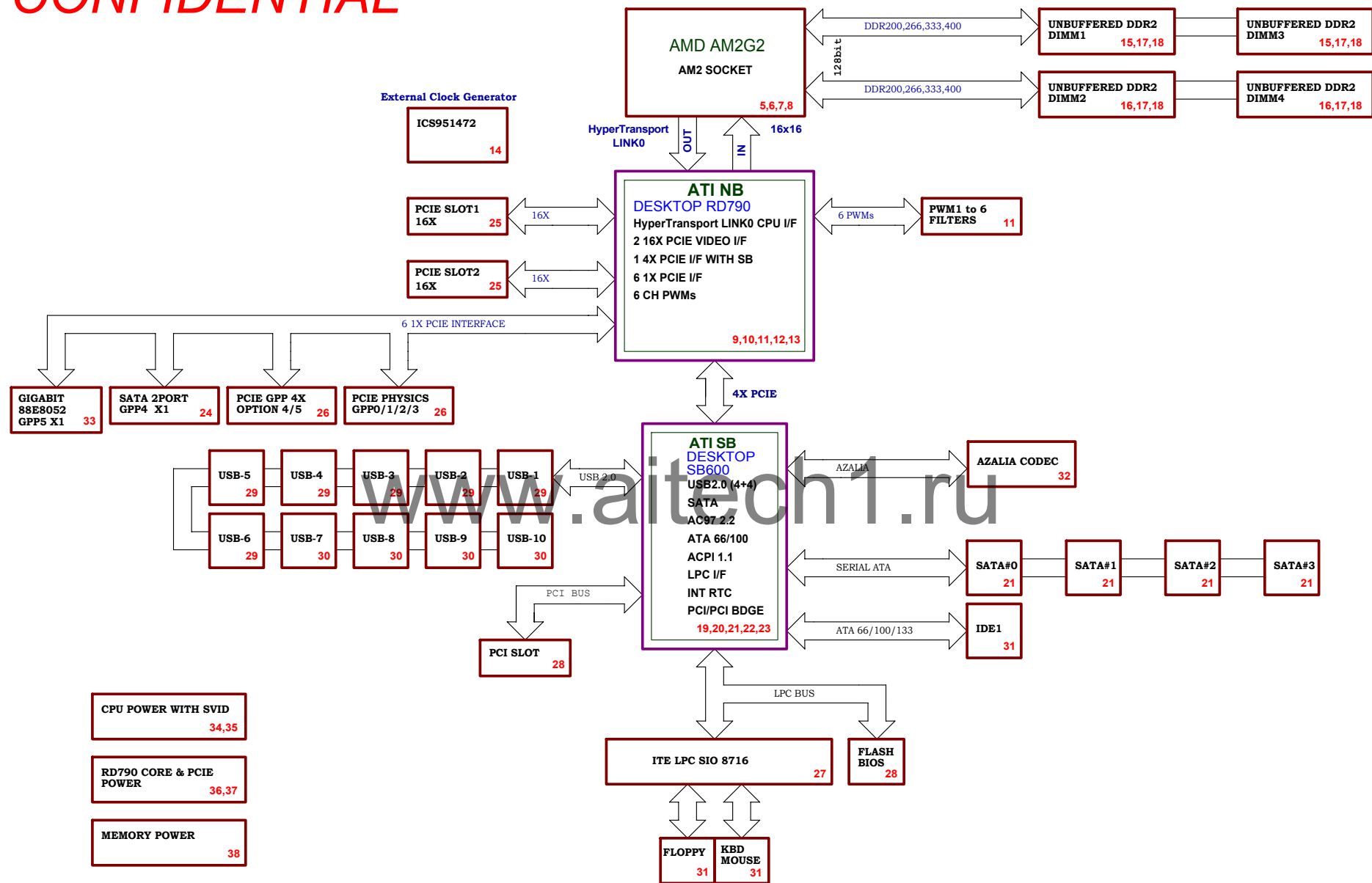
SHEET TITLE

26	CODEC ALC889 , F AUDIO
27	AUDIO JACK
28	ITE 8718 (GB)
29	KB/MS , H/W MONITOR & FAN CONTROL
30	ATX POWER CONNCTOR
31	REALTEK RTL8111B/C
32	JMB363
33	JMB363 ESATA
34	TI TSB43AB23 1394A
35	PWM - ISL6323
36	PWM - MOS,CHOKE
37	POWER SEQUENCE
38	NB POWER , VCC12HT , VDDA25
39	DDRII POWER , VCC18
40	DUAL BIOS+
41	
42	
43	
44	
45	
46	

GIGABYTE CORP.

BLOCK DIAGRAM			
Size	Document Number	Rev	
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Date:	Friday, September 14, 2007	Sheet	1 of 40

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GIGABYTE CORP.

BLOCK DIAGRAM			
Title	Document Number	Rev	
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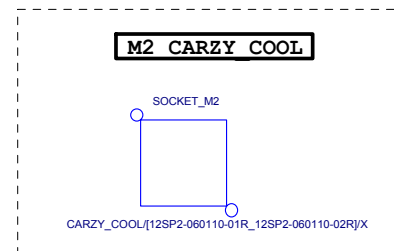
L0_CADIN_L[0..15] <L0_CADIN_L[0..15] [11]
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] [11]
L0_CLKIN_L[0..1] <L0_CLKIN_L[0..1] [11]
L0_CLKIN_H[0..1] <L0_CLKIN_H[0..1] [11]
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] [11]
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] [11]
L0_CLKOUT_L[0..1] <L0_CLKOUT_L[0..1] [11]
L0_CLKOUT_H[0..1] <L0_CLKOUT_H[0..1] [11]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

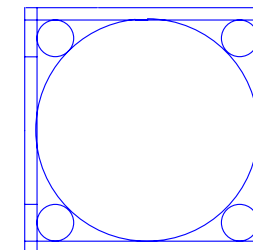
VLDT_A = VCC12_HT
VLDT_B = HT12B



CPU-SK/940AM2/S/15u[10SC1-A01940-11R_10SC1-A01940-14R]

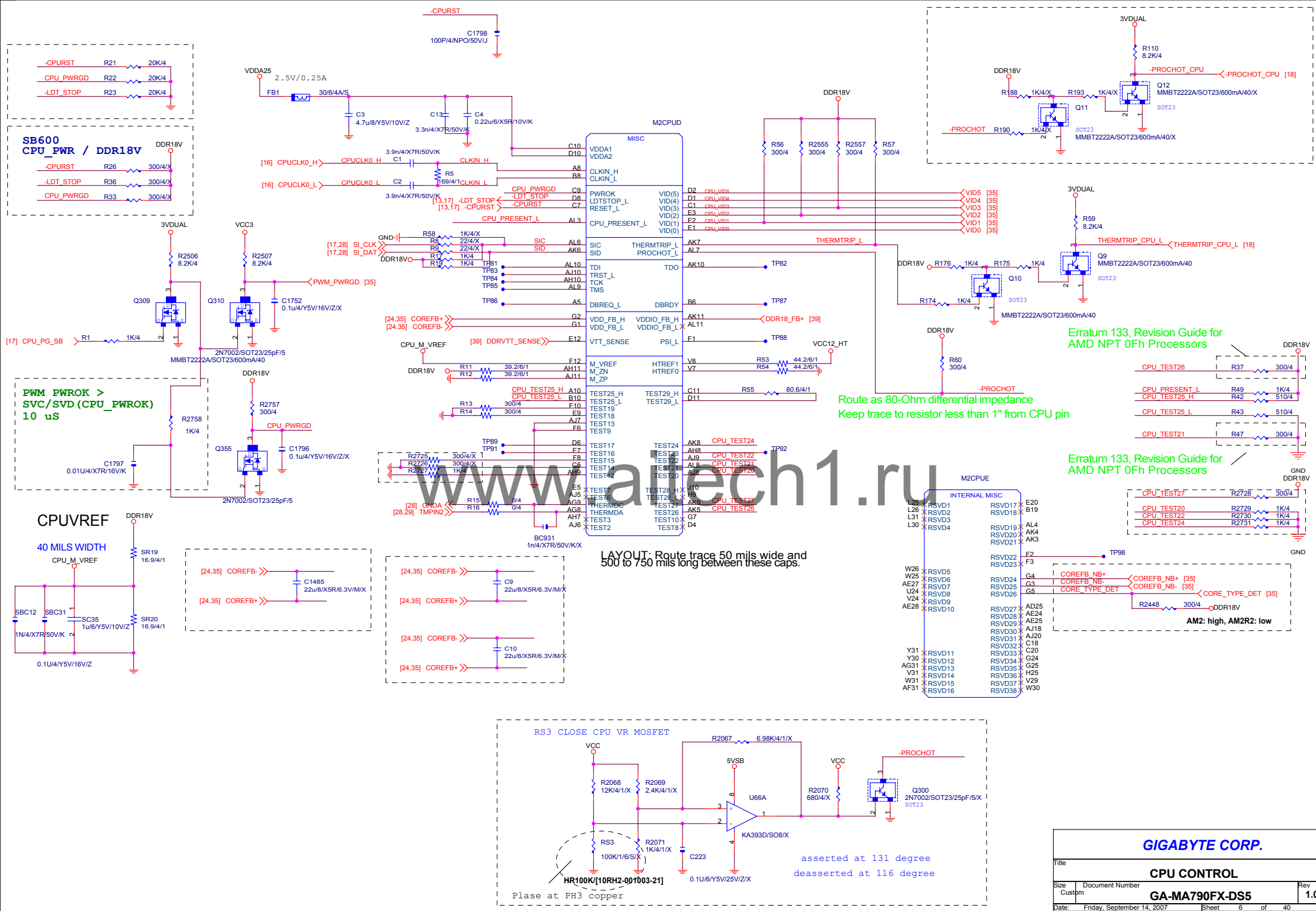


SOCKET_M2
M2_RM/PLASTICS[12KRC-04K807-42R_12KRC-04K807-43R]

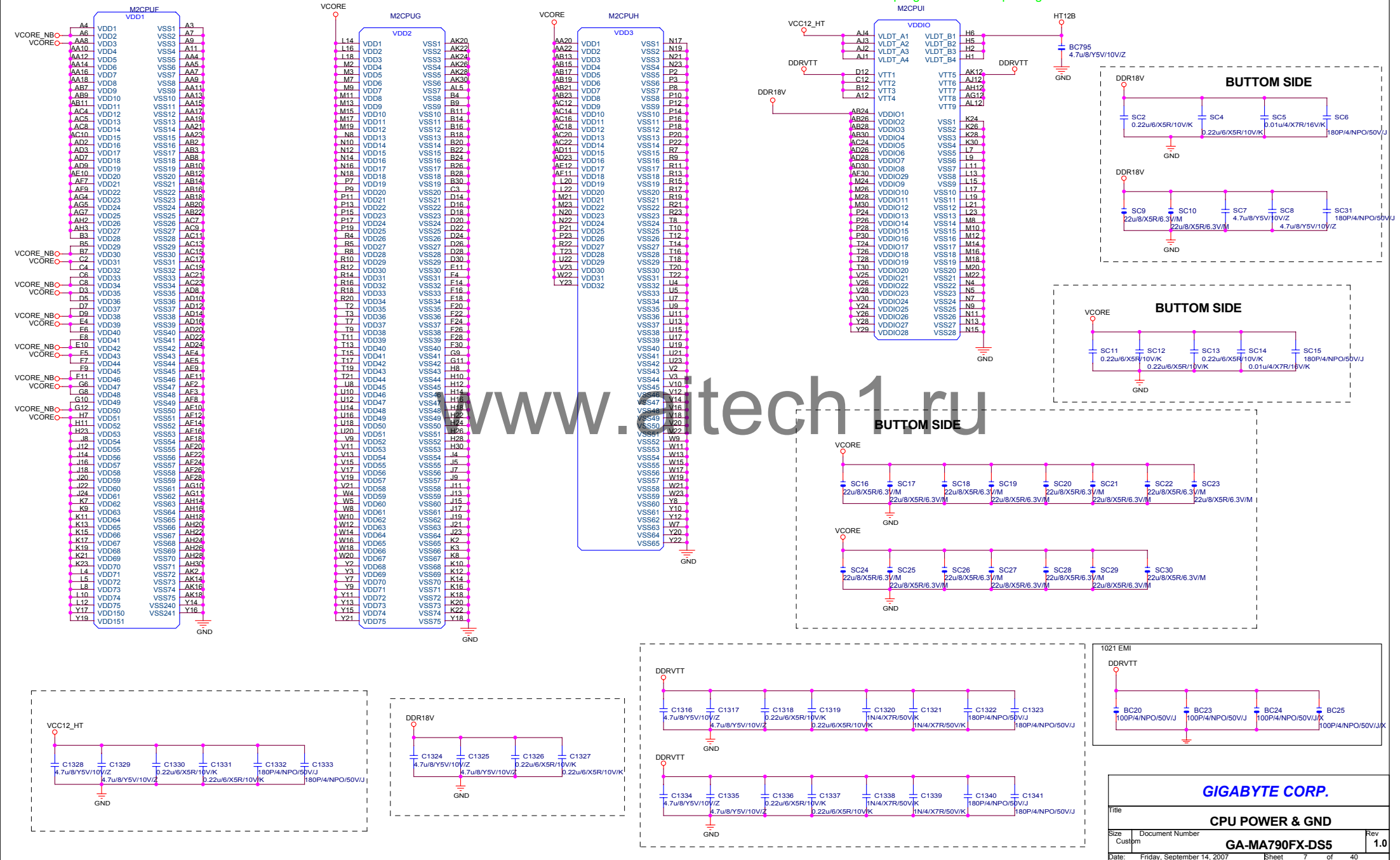


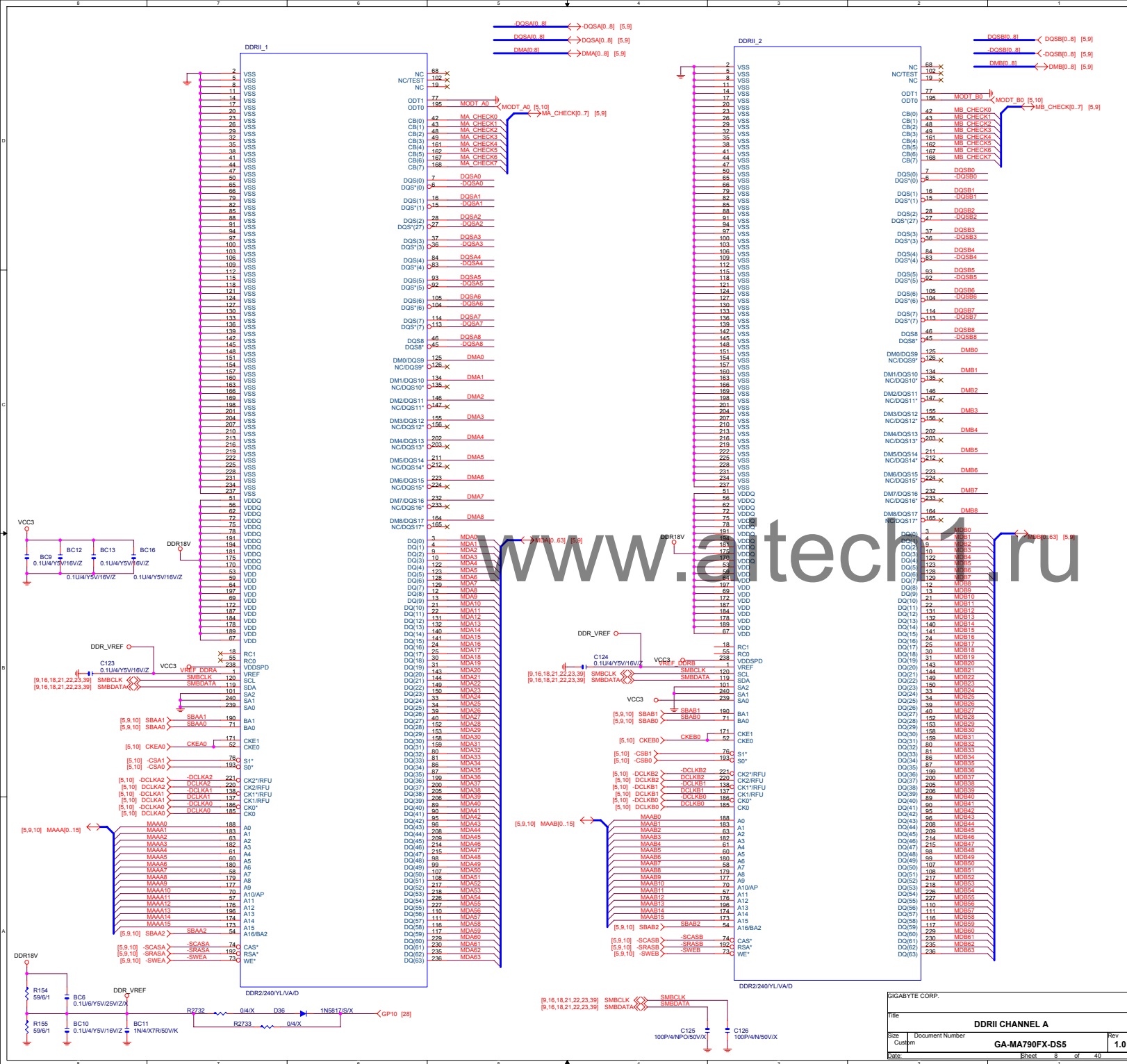
GIGABYTE CORP.

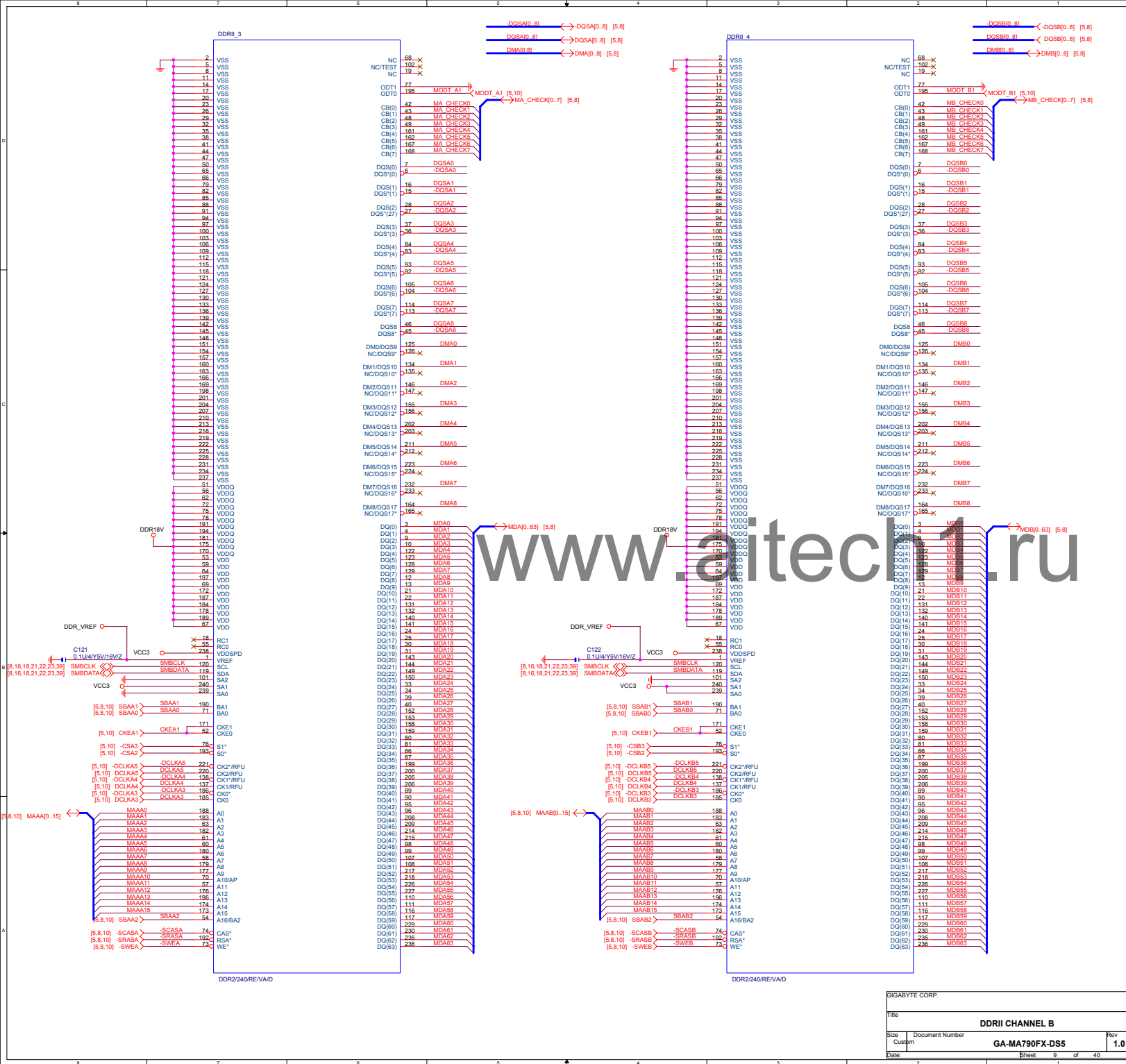
Title				
CPU HYPER TRANSPORT				
Size	Document Number			Rev
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VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.







[4] L0_CADOUT_H0_15] < L0_CADOUT_H0_15] [4]
[4] L0_CADOUT_L0_15] < L0_CADOUT_L0_15] [4]

EXP A_RXP0_15] >> EXP_A_RXP0_15] [21]
EXP A_RXN0_15] >> EXP_A_RXN0_15] [21]

EXP A_TXP0_15] >> EXP_A_TXP0_15] [21]
EXP A_TXN0_15] >> EXP_A_TXN0_15] [21]

[4] L0_CLKOUT_H1] >> L0_CLKOUT_H1] [4]
[4] L0_CLKOUT_L1] >> L0_CLKOUT_L1] [4]
[4] L0_CLKOUT_H0] >> L0_CLKOUT_H0] [4]
[4] L0_CLKOUT_L0] >> L0_CLKOUT_L0] [4]
[4] L0_CTLOUT_H1] >> L0_CTLOUT_H1] [4]
[4] L0_CTLOUT_L1] >> L0_CTLOUT_L1] [4]
[4] L0_CTLOUT_H0] >> L0_CTLOUT_H0] [4]
[4] L0_CTLOUT_L0] >> L0_CTLOUT_L0] [4]

R2350 1.21K/41 HT_RXCALN A29 HT_RXCALP B29 HT_RXCALN
HT_RXCALN

EXP A_RXP0 B7 GFX_RX0P
EXP A_RXN0 A6 GFX_RX0N
EXP A_RXP1 B4 GFX_RX1P
EXP A_RXN1 A4 GFX_RX1N
EXP A_RXP2 G12 GFX_RX2P
EXP A_RXN2 H12 GFX_RX2N
EXP A_RXP3 F9 GFX_RX3P
EXP A_RXN3 G11 GFX_RX3N
EXP A_RXP4 C11 GFX_RX4P
EXP A_RXN4 D11 GFX_RX4N
EXP A_RXP5 F2 GFX_RX5P
EXP A_RXN5 F1 GFX_RX5N
EXP A_RXP6 H2 GFX_RX6P
EXP A_RXN6 H1 GFX_RX6N
EXP A_RXP7 L2 GFX_RX7P
EXP A_RXN7 L1 GFX_RX7N

EXP A_RXP8 L8 GFX_RX8P
EXP A_RXN8 L7 GFX_RX8N
EXP A_RXP9 L5 GFX_RX9P
EXP A_RXN9 M5 GFX_RX9N
EXP A_RXP10 M2 GFX_RX10P
EXP A_RXN10 N1 GFX_RX10N
EXP A_RXP11 P1 GFX_RX11P
EXP A_RXN11 P2 GFX_RX11N
EXP A_RXP12 R2 GFX_RX12P
EXP A_RXN12 R1 GFX_RX12N
EXP A_RXP13 U9 GFX_RX13P
EXP A_RXN13 U8 GFX_RX13N
EXP A_RXP14 V1 GFX_RX14P
EXP A_RXN14 T2 GFX_RX14N
EXP A_RXP15 W2 GFX_RX15P
EXP A_RXN15 W1 GFX_RX15N

U170A

PART 1/5

HYPERTRANSPORT
I/F

PCIE GFX
I/F

115R0DA/AA12FGS

HT_TXCAD15P R28 L0_CADIN_H15
HT_TXCAD15N R29 L0_CADIN_L15
HT_TXCAD14P M26 L0_CADIN_H14
HT_TXCAD14N M25 L0_CADIN_L14
HT_TXCAD13P N28 L0_CADIN_H13
HT_TXCAD13N N27 L0_CADIN_L13
HT_TXCAD12P M28 L0_CADIN_H12
HT_TXCAD12N M29 L0_CADIN_L12
HT_TXCAD11P J27 L0_CADIN_H11
HT_TXCAD11N J26 L0_CADIN_L11
HT_TXCAD10P J29 L0_CADIN_H10
HT_TXCAD10N J28 L0_CADIN_L10
HT_TXCAD10P H29 L0_CADIN_H9
HT_TXCAD10N H28 L0_CADIN_L9
HT_TXCAD9P F30 L0_CADIN_H8
HT_TXCAD9N F29 L0_CADIN_L8
HT_TXCAD8P N33 L0_CADIN_H7
HT_TXCAD8N N32 L0_CADIN_L7
HT_TXCAD7P M33 L0_CADIN_H6
HT_TXCAD7N M32 L0_CADIN_L6
HT_TXCAD6P K33 L0_CADIN_H5
HT_TXCAD6N K32 L0_CADIN_L5
HT_TXCAD5P L32 L0_CADIN_L4
HT_TXCAD5N J32 L0_CADIN_L4
HT_TXCAD4P F33 L0_CADIN_H3
HT_TXCAD4N G32 L0_CADIN_L3
HT_TXCAD3P E33 L0_CADIN_H2
HT_TXCAD3N E32 L0_CADIN_L2
HT_TXCAD2P D33 L0_CADIN_H1
HT_TXCAD2N D32 L0_CADIN_L1
HT_TXCAD1P C33 L0_CADIN_H0
HT_TXCAD1N C32 L0_CADIN_L0
HT_TXCAD0P L27 L0_CLKIN_L1
HT_TXCAD0N L28 L0_CLKIN_H1
HT_TXCLK1P H33 L0_CLKIN_L0
HT_TXCLK1N H32 L0_CLKIN_H0

[4] L0_CLKIN_L1] >> L0_CLKIN_L1] [4] swap P/N due
[4] L0_CLKIN_H1] >> L0_CLKIN_H1] [4] to mislabel
[4] L0_CLKIN_L0] >> L0_CLKIN_L0] [4]
[4] L0_CLKIN_H0] >> L0_CLKIN_H0] [4]

HT_TXCTL1P R26 L0_CTLIN_H1
HT_TXCTL1N R25 L0_CTLIN_L1
HT_TXCTL0P P33 L0_CTLIN_H0
HT_TXCTL0N P32 L0_CTLIN_L0

HT_TXCALP A28 HT_TXCALN R2351 1.21K/41
HT_TXCALN

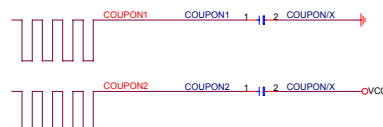
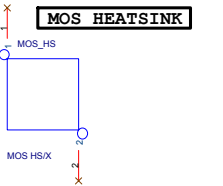
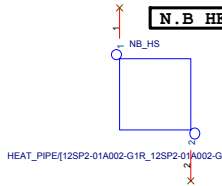
EXP A_TXP0 A8
EXP A_TXN0 B8
EXP A_TXP1 B5
EXP A_TXN1 A5
EXP A_TXP2 C9
EXP A_TXN2 E9
EXP A_TXP3 H11
EXP A_TXN3 H6
EXP A_TXP4 J9
EXP A_TXN4 J5
EXP A_TXP5 D2
EXP A_TXN5 E1
EXP A_TXP6 G2
EXP A_TXN6 G1
EXP A_TXP7 K2
EXP A_TXN7 K1

EXP A_TXP8 J6
EXP A_TXN8 J5
EXP A_TXP9 L2
EXP A_TXN9 L3
EXP A_TXP10 N6
EXP A_TXN10 N7
EXP A_TXP11 N5
EXP A_TXN11 M6
EXP A_TXP12 R6
EXP A_TXN12 R5
EXP A_TXP13 R8
EXP A_TXN13 R9
EXP A_TXP14 U6
EXP A_TXN14 U5
EXP A_TXP15 W6
EXP A_TXN15 W5

PLACE THESE CAP CLOSE
TO CONNECTOR

N.B HEATSINK

MOS HEATSINK







[13] DFT_GPIO5 << R2391 1K/4/X

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using
nbcfg register access)
0 : Enable

[13] DFT_GPIO4 << R2392 1K/4

[13] DFT_GPIO3 << R2393 1K/4/X

[13] DFT_GPIO2 << R2394 1K/4

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
(GPIO4 , GPIO3 , GPIO2)
000 : 00001 (4 + 2)
001 : 00010 (4 + 1 + 1)
010 : 01011 (1 + 1 + 1 + 1 + 1 + 1)
011 : 00100 (2 + 1 + 1 + 1 + 1)
100 : 01010 (2 + 2 + 1 + 1)
101 : 01100 (2 + 2 + 2)
111 : 01011 (1 + 1 + 1 + 1 + 1 + 1) or EEPROM

[13] DFT_GPIO1 << R2395 1K/4/X

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected

[13] DFT_GPIO0 << R2396 1K/4/X

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

[13] DBG_GPIO0 << 1 TP115

[13] DBG_GPIO1 << 1 TP116

[13] DBG_GPIO2 << 1 TP117

[13] DBG_GPIO3 << 1 TP118

All of the above straps are active low straps and are pulled
up internally to work in default states. It is not required to
connect any external pull up to these straps. In order to
change the default values of the strap, the strap pins must
be pulled down to VSS through a resistor (typically 3 Kohm).

GIGABYTE CORP.

Title

RD790 STRAPS

Size
B

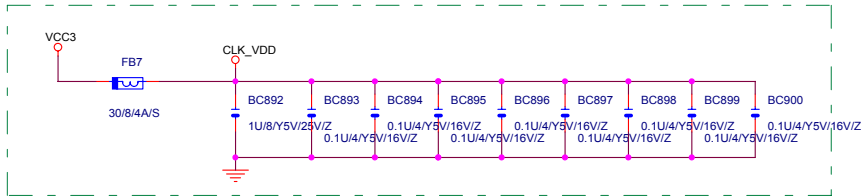
Document Number

GA-MA790FX-DS5

Rev
1.0

Date:

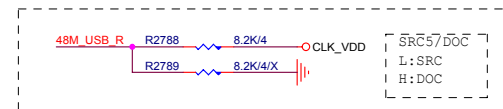
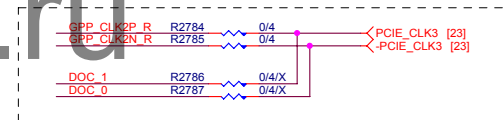
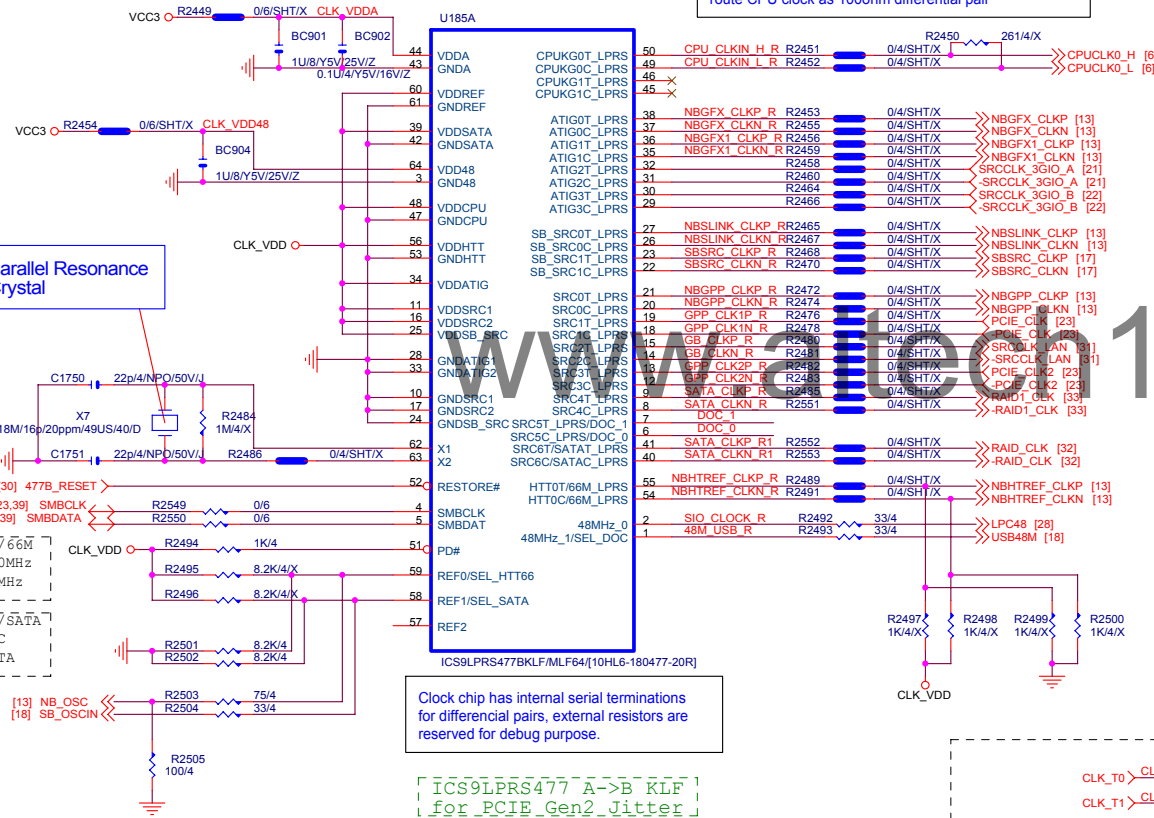
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- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

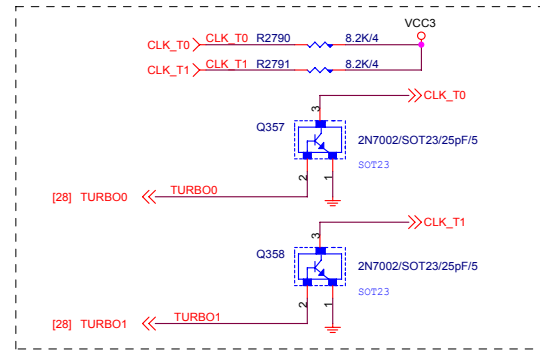
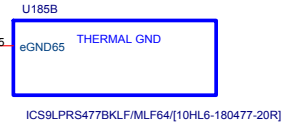


Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

[ICS9LPRS477 A->B KLF]
for PCIe Gen2 Jitter

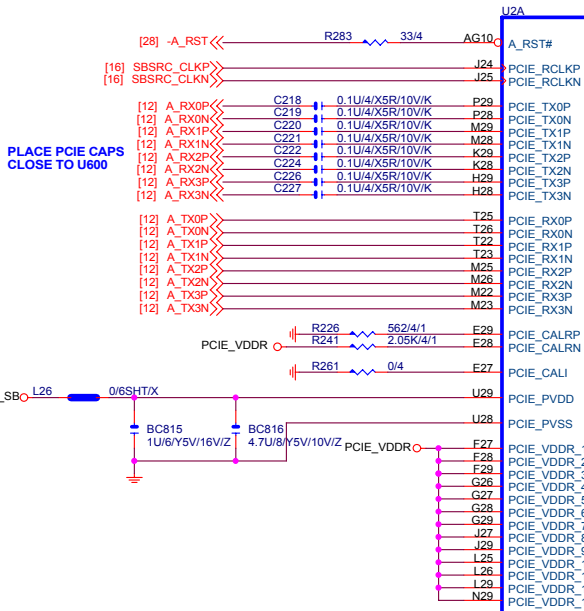
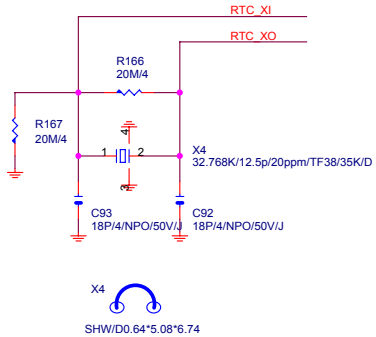
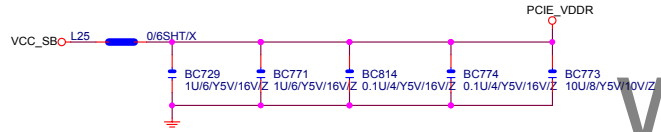
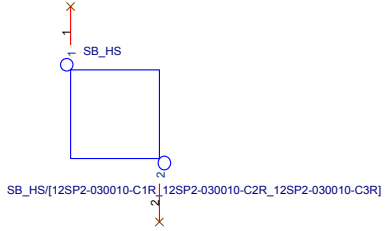


GIGABYTE CORP.

Title		
ICS9LPRS472		
Size	Document Number	Rev
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SB CALIBRATION RESISTOR VALUE	
SB600	
R601	562 OHM 1%
R602	2.05K 1%
R603	0R

S.B HEATSINK



SB600 SB 23x23mm

Part 1 of 4

PCI EXPRESS INTERFACE

PCI INTERFACE

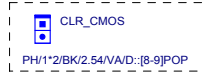
CPU

RTC

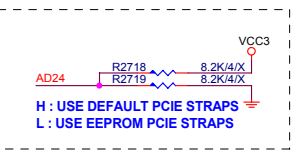
CLR_CMOS

NOT ADD ICT FOR RTCVDD PIN

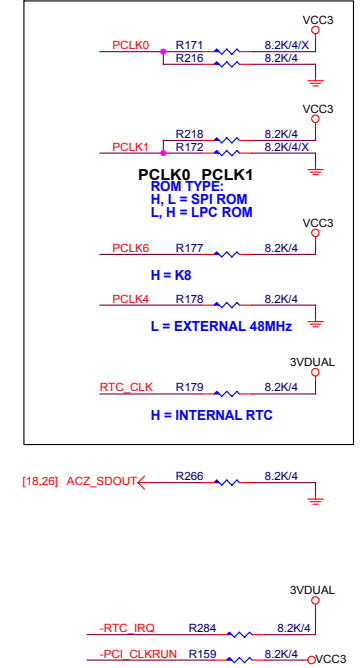
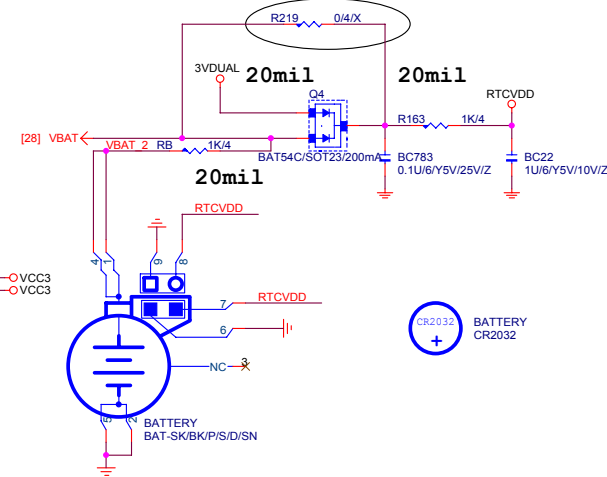
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL



[23,34] AD[0..31] <-->

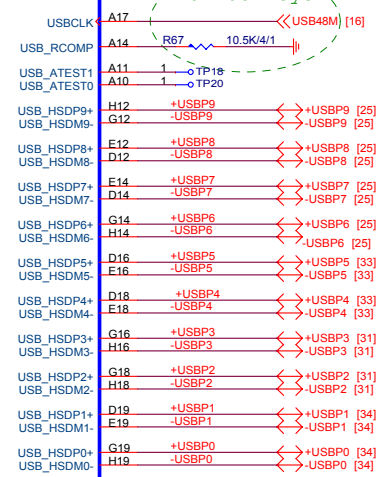
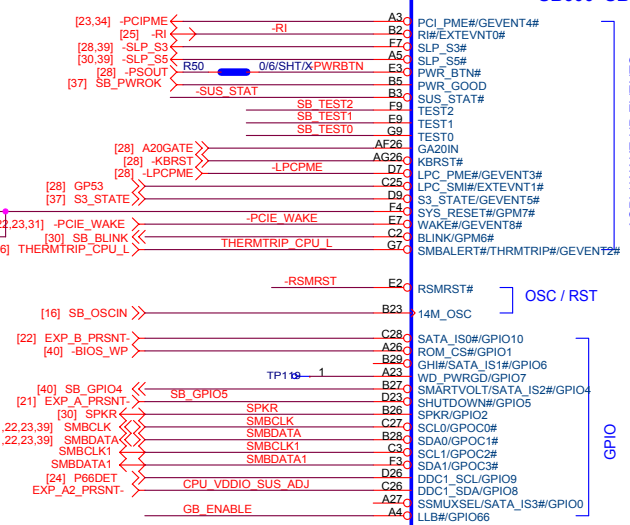
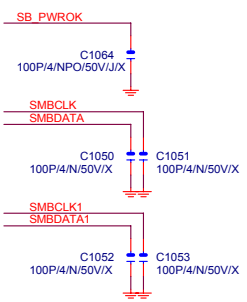
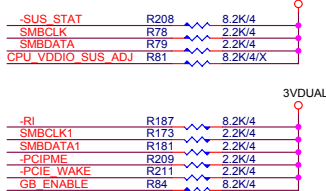
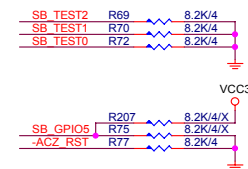


ATI Anthony recommend

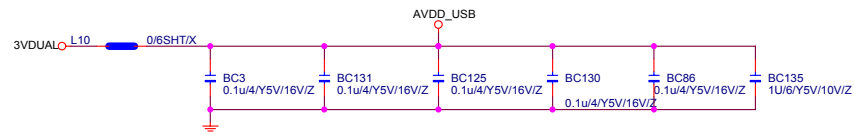
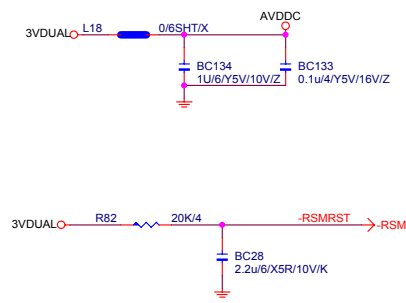


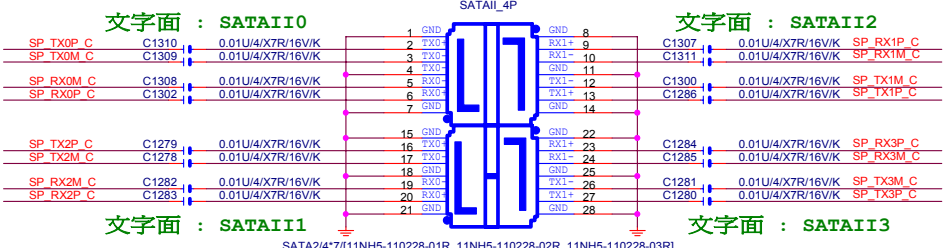
GIGABYTE CORP.

Title		
ATI SB600-PCIW/PCI/CPU/LPC		
Size	Document Number	Rev
Custom	GA-MA790FX-DS5	1.0
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- USB9 FRONT PANEL (SB600 ONLY)
- USB8 FRONT PANEL (SB600 ONLY)
- USB7 FRONT PANEL
- USB6 FRONT PANEL
- USB5 USB ESATA
- USB4 USB ESATA
- USB3 LAN USB BOTTOM
- USB2 LAN USB TOP
- USB1 LAN USB BOTTOM
- USB0 LAN USB TOP

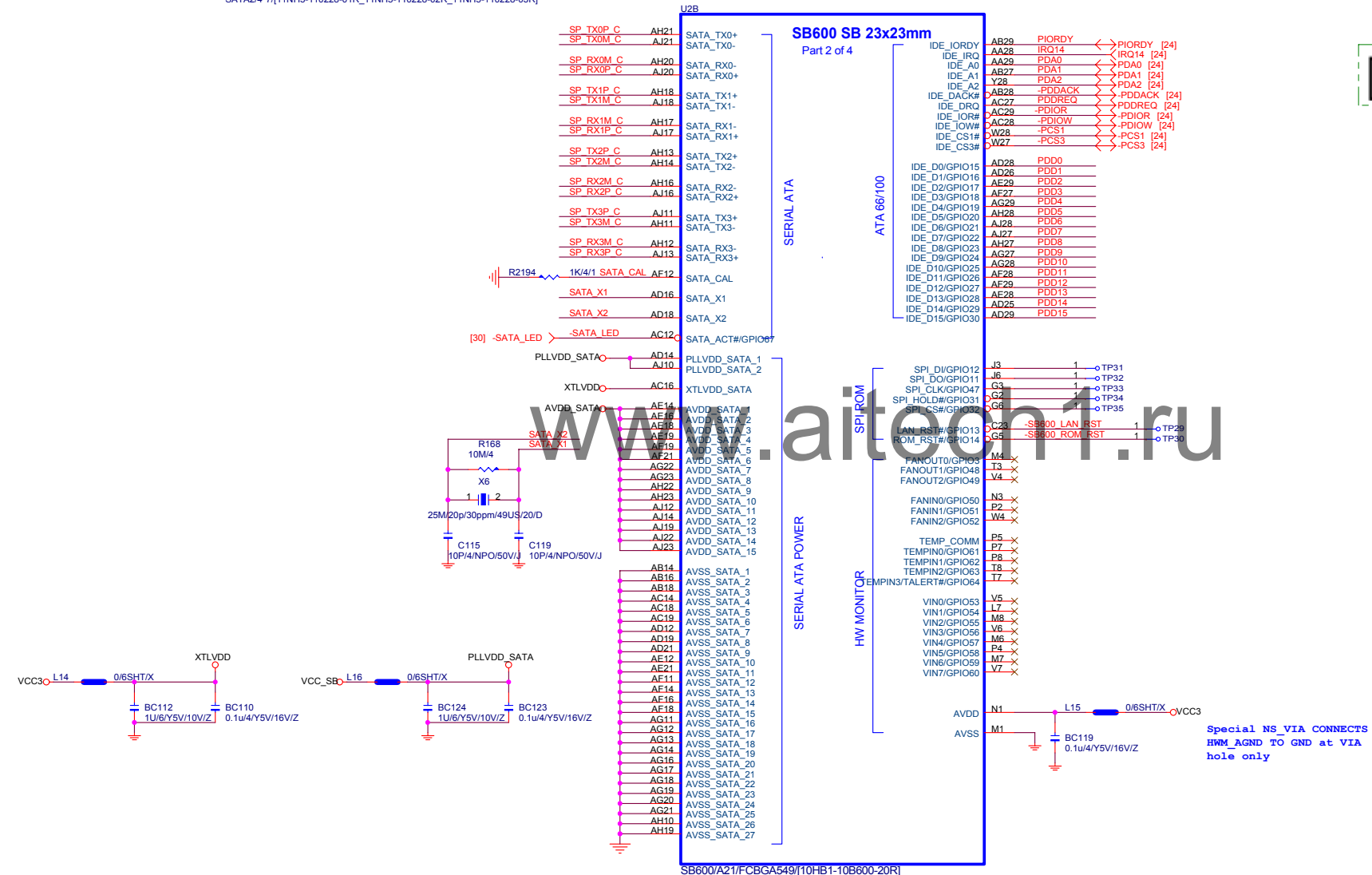
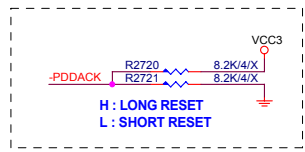




PLACE SATA AC COUPLING CAPS CLOSE TO SB600

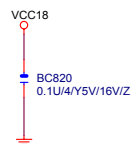
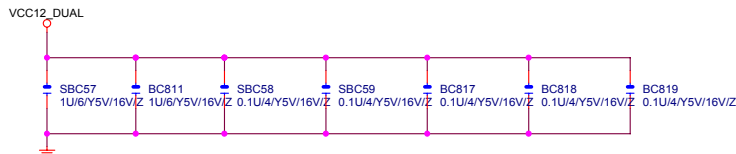
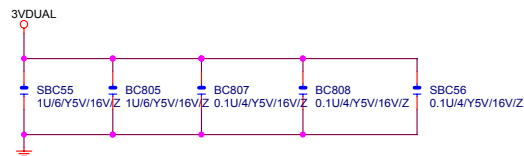
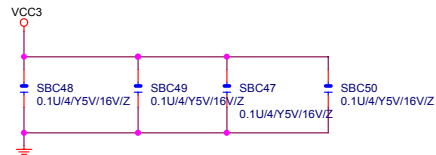
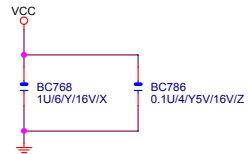
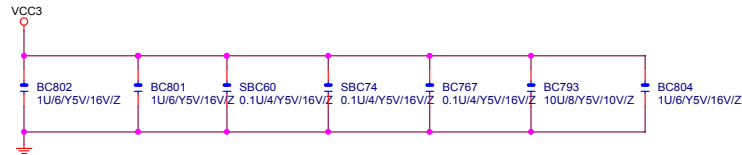
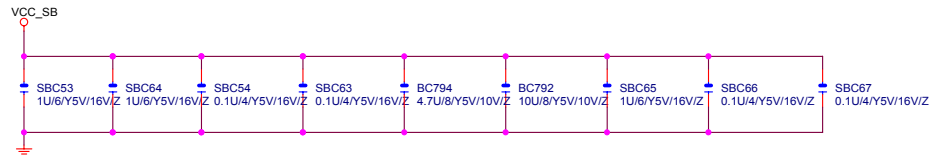


NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE

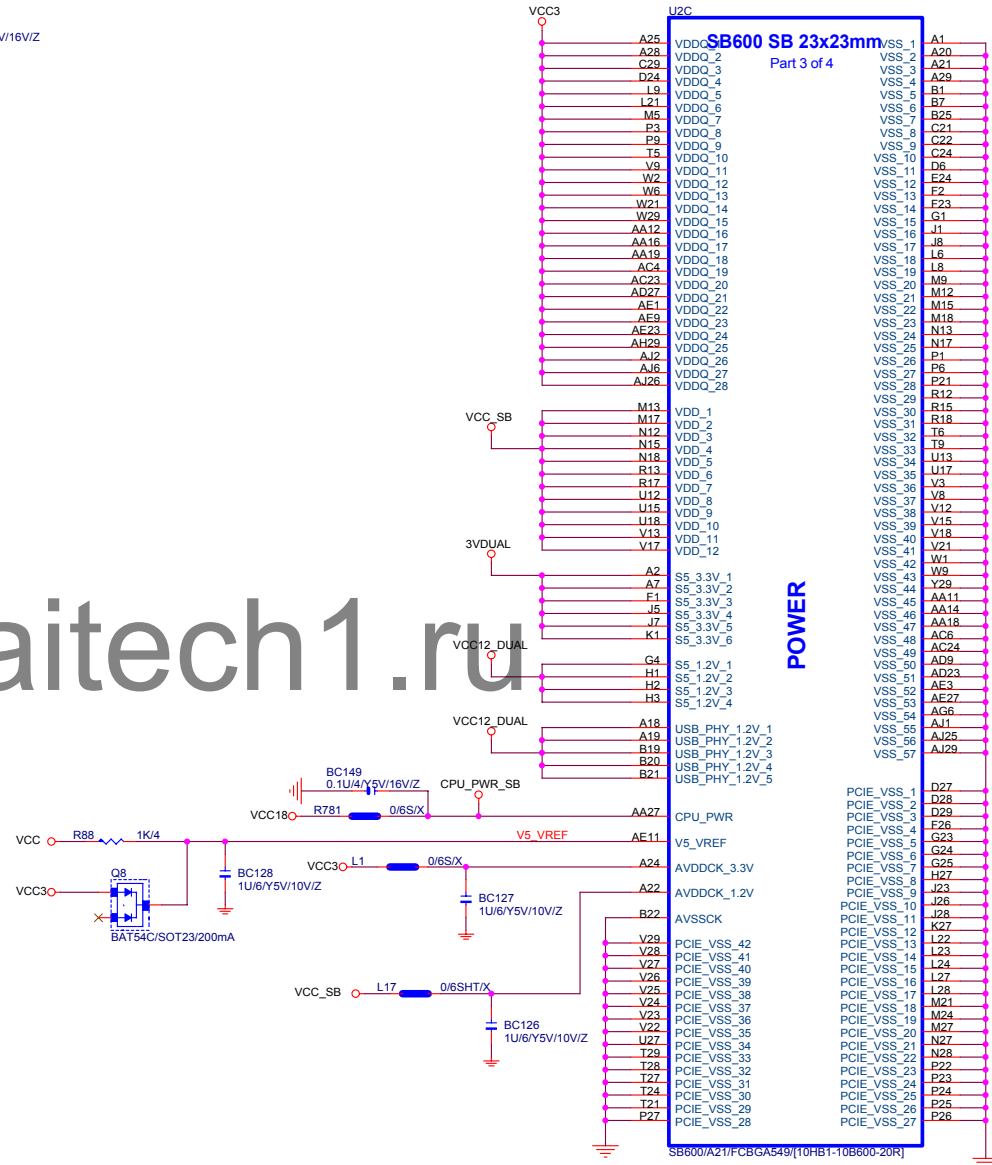


Special NS_VIA CONNECTS HWM_AGND TO GND at VIA hole only

GIGABYTE CORP.			
Title			
ATI SB600-SATA,PDD,IDE,HWM			
Size	Document Number	Rev	
Custom	GA-MA790FX-DS5	1.0	
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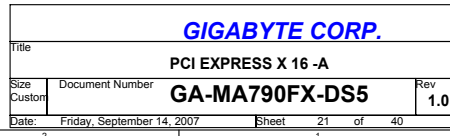


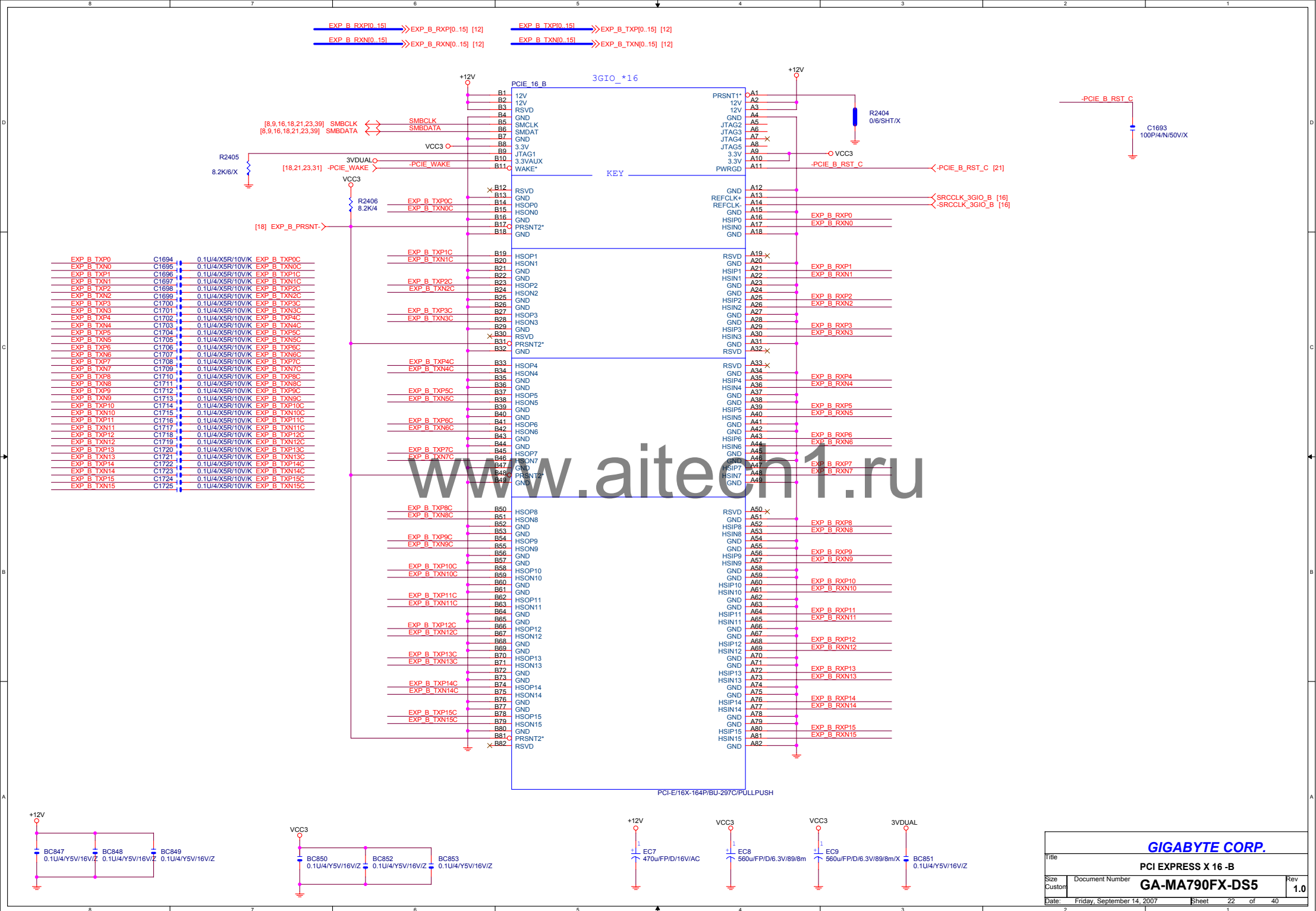
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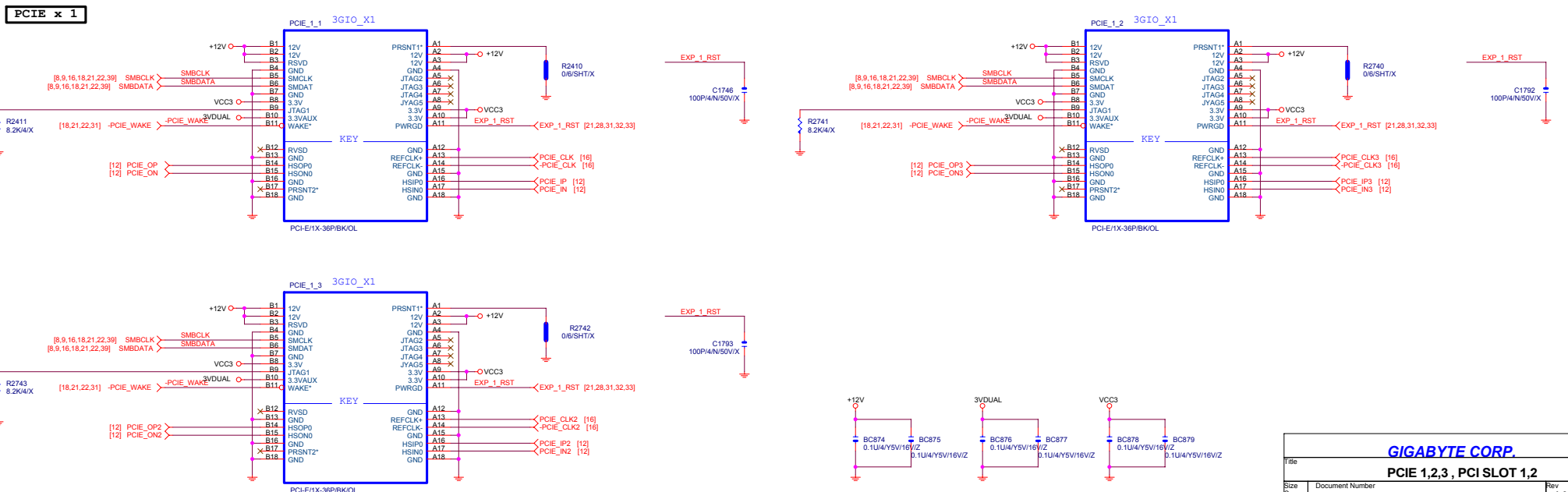
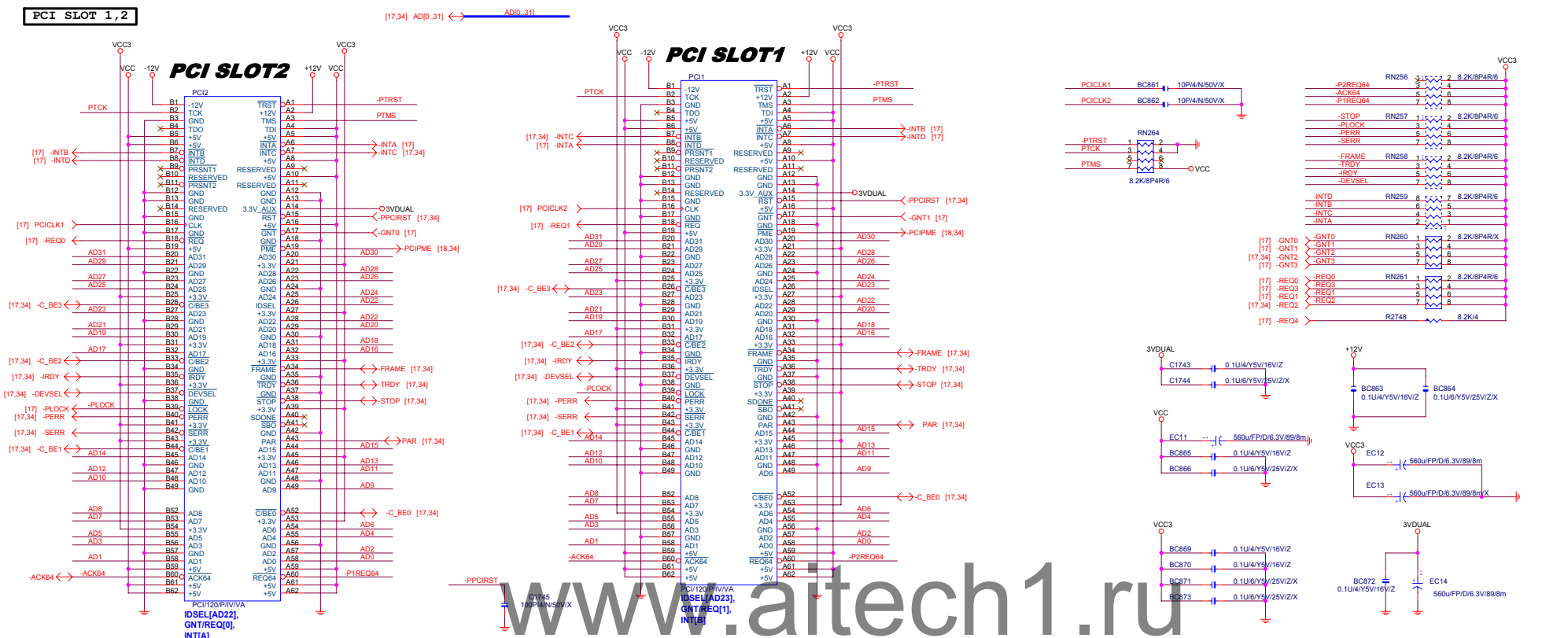


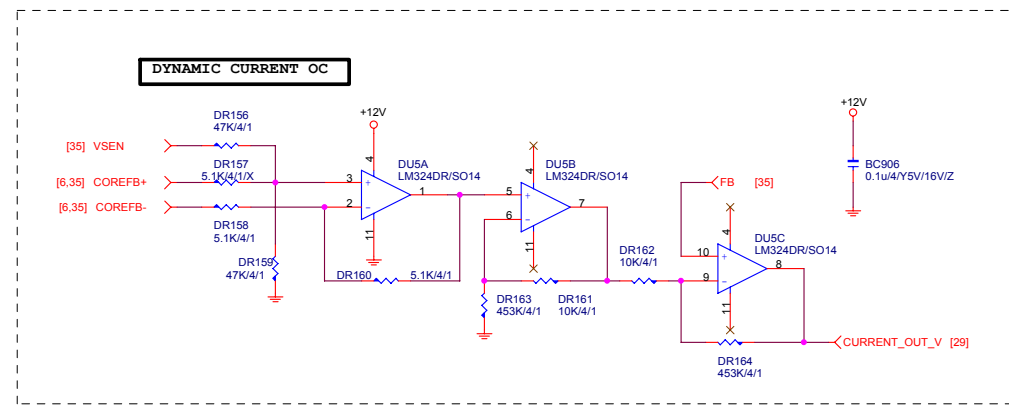
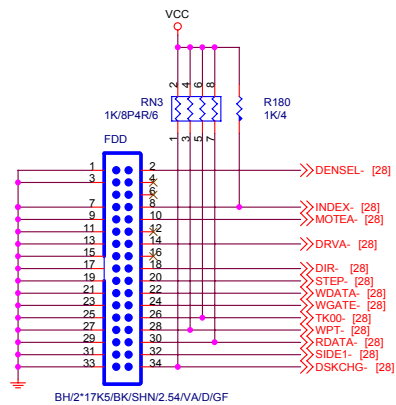
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Custom				1.0
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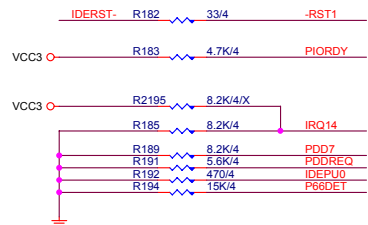




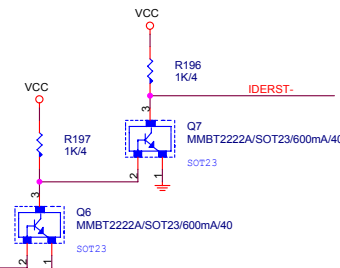
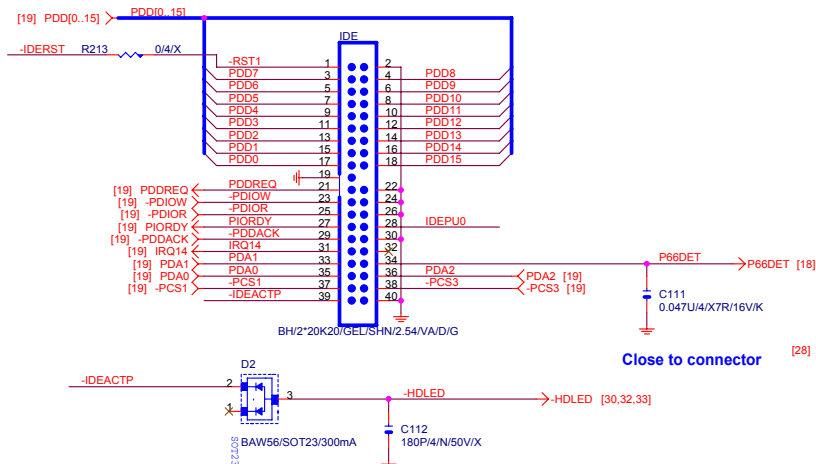




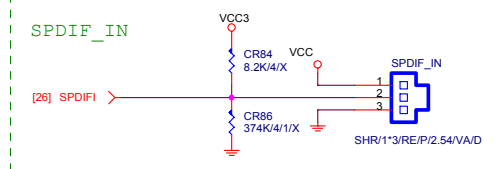
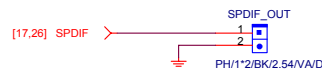
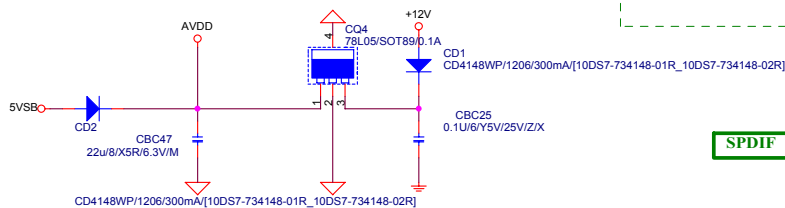
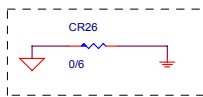
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PRIMARY IDE CONNECTOR



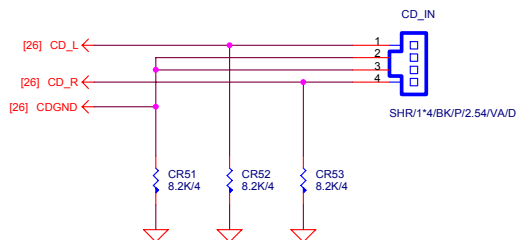
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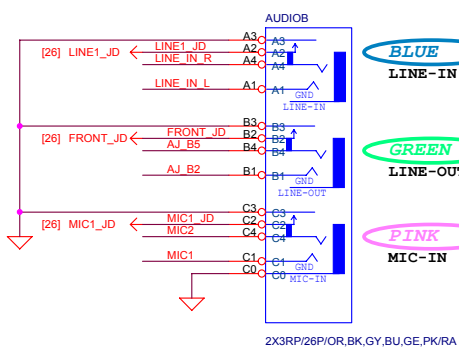
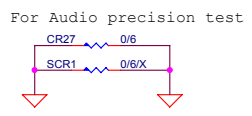
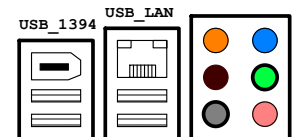
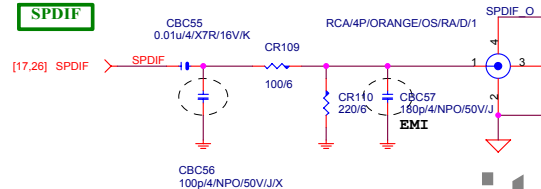
SPDIF



CD IN



SPDIF



BLUE

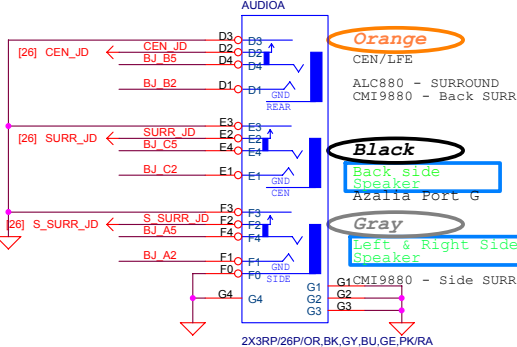
LINE-IN

GREEN

LINE-OUT

PINK

MIC-IN



Orange

ALC880 - SURROUND

CM19880 - Back SURR

Black

Back side Speaker

Azalia Port G

Gray

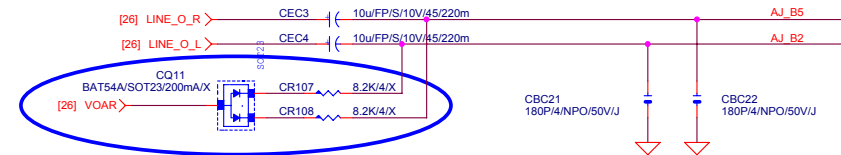
Left & Right Side Speaker

CM19880 - Side SURR

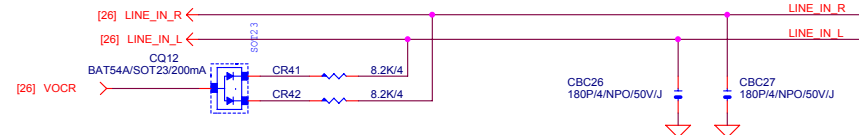
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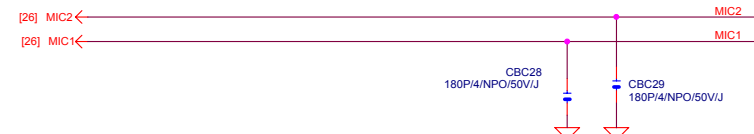
**LINE OUT
FRONT OUT**



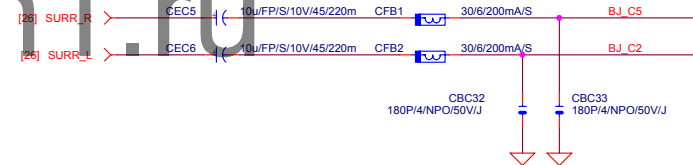
LINE-IN



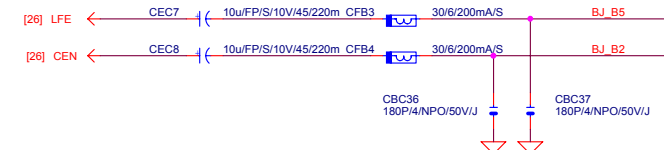
MIC



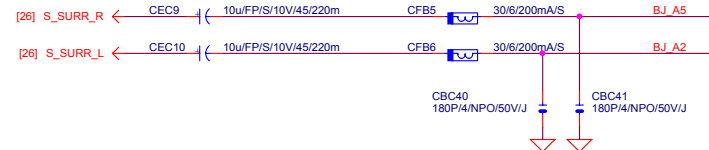
SURROUND



CEN/LFE

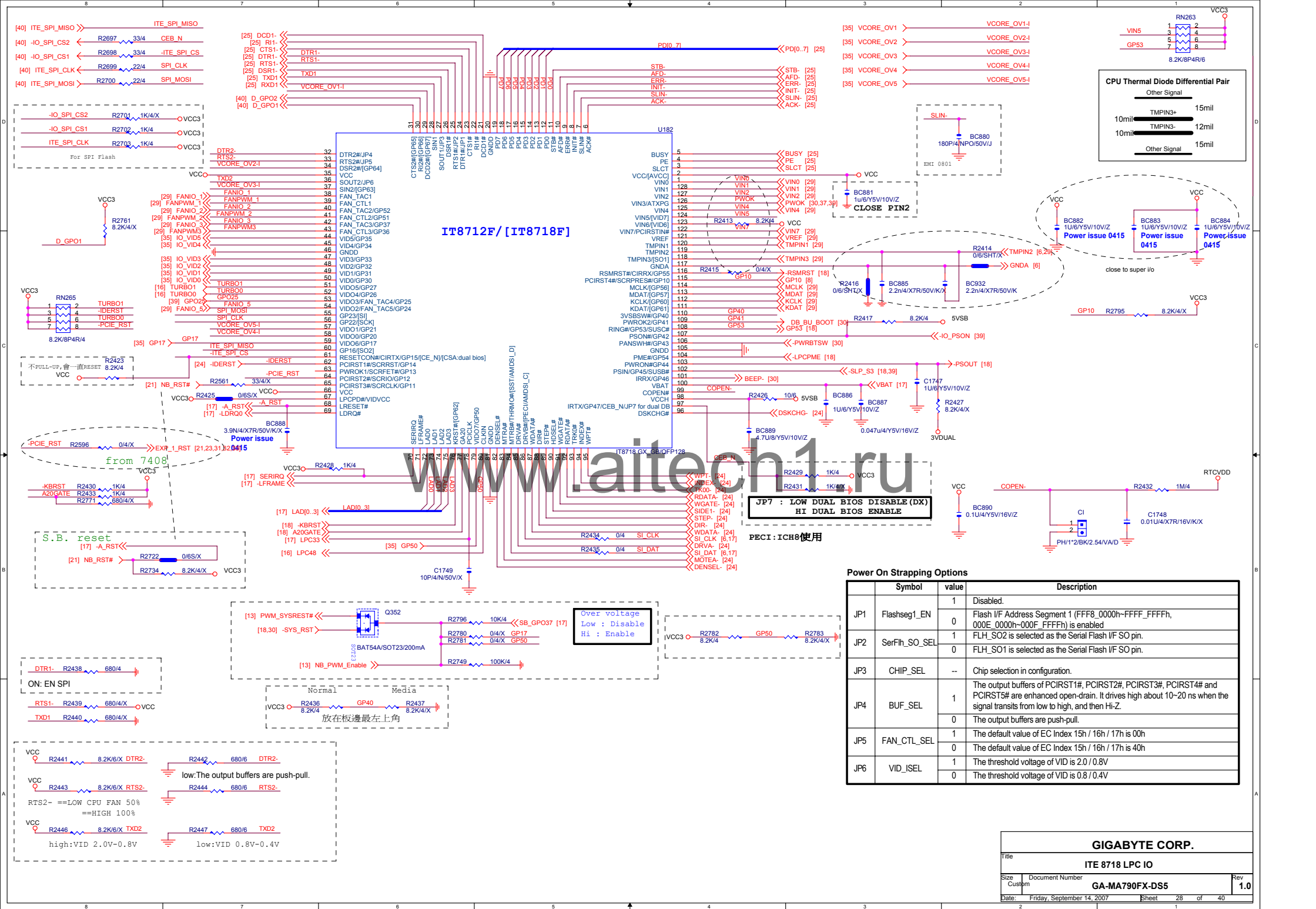


SURR BACK

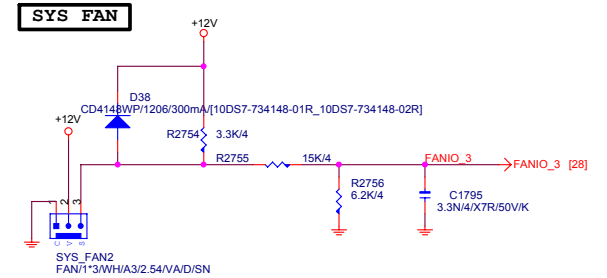
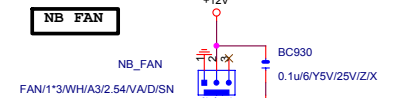
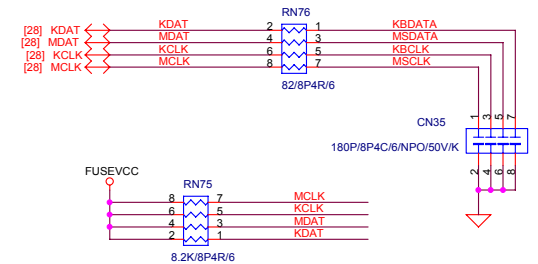
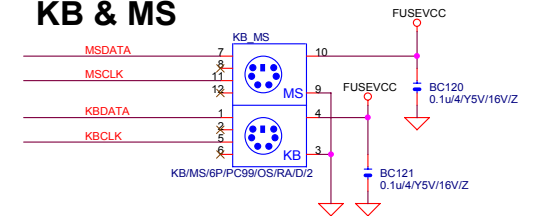
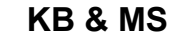
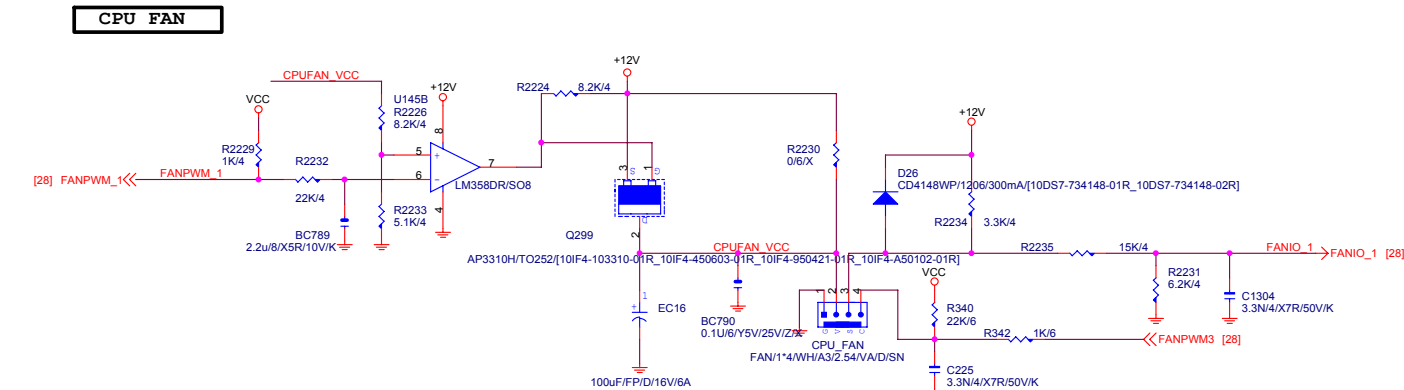
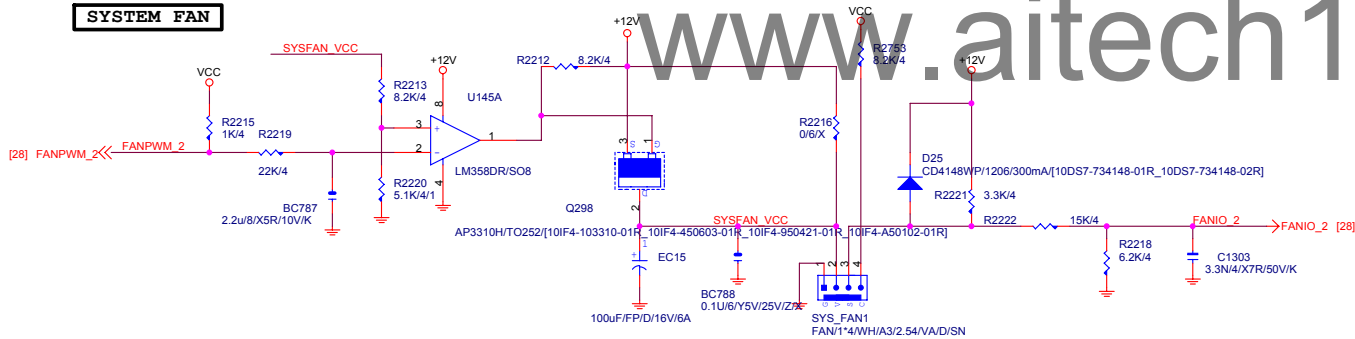
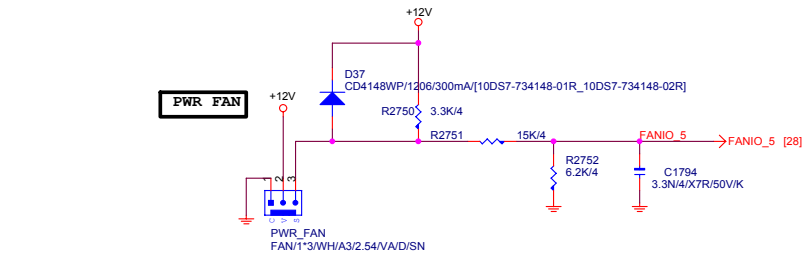
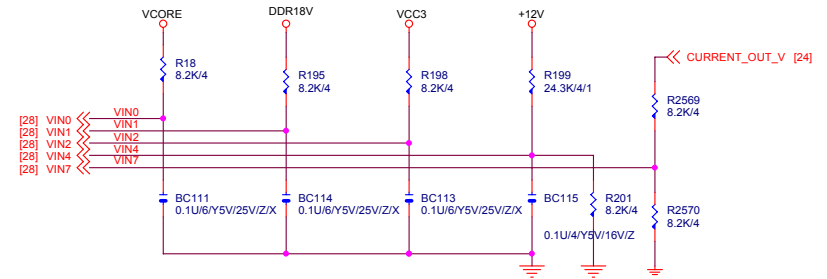
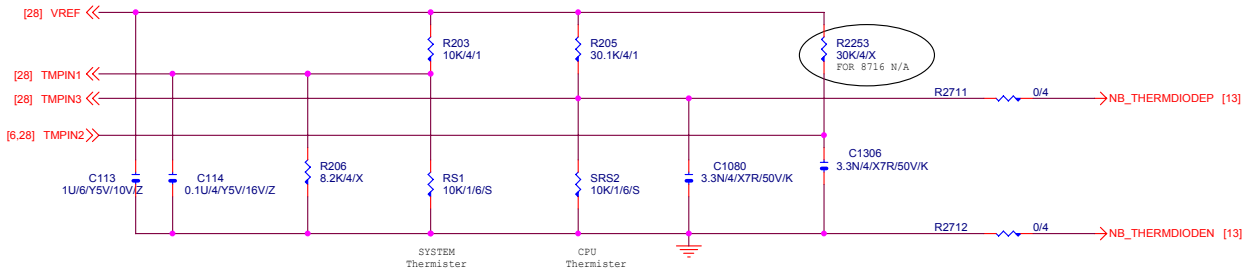


GIGABYTE CORP.

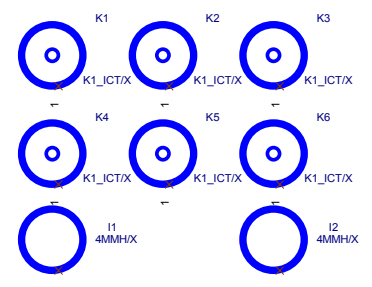
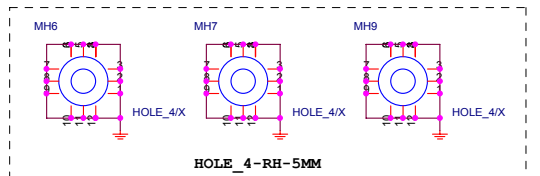
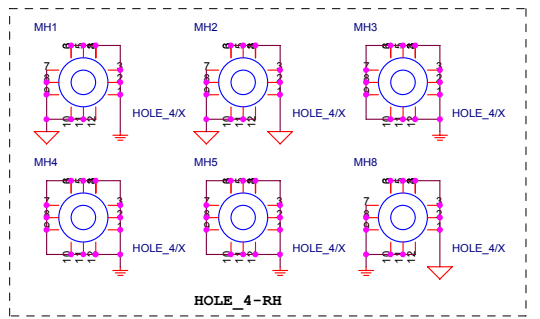
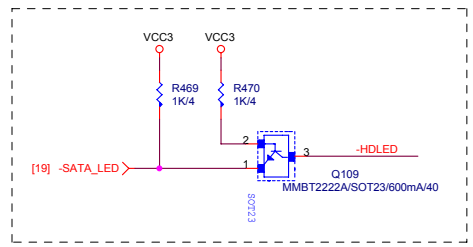
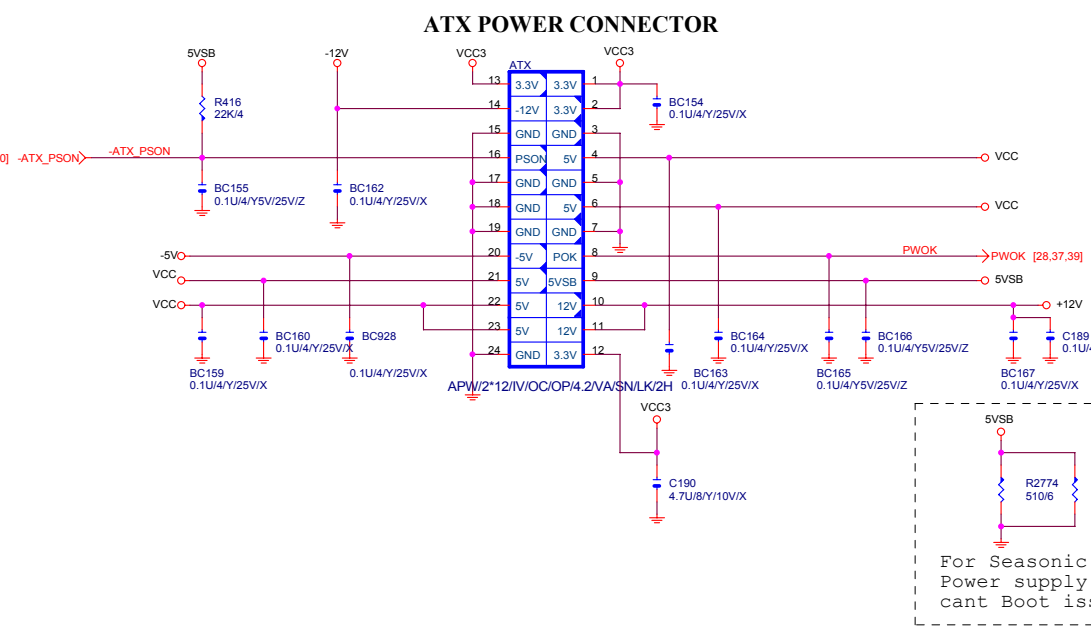
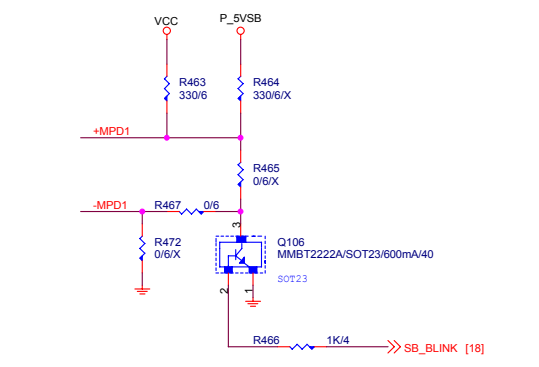
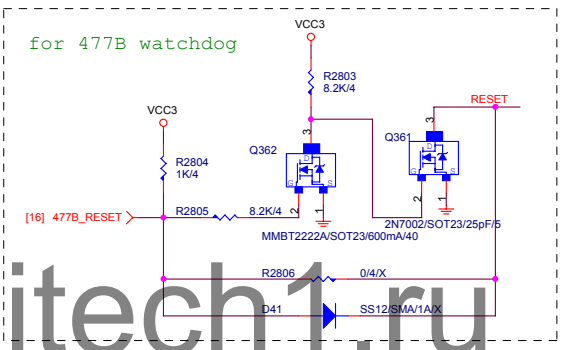
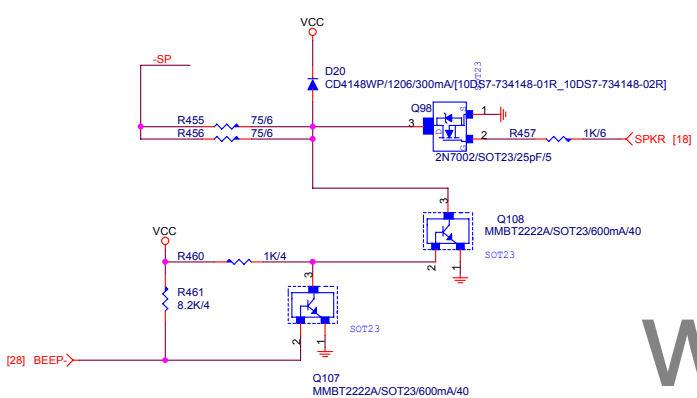
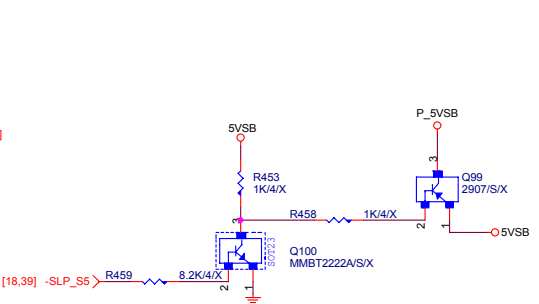
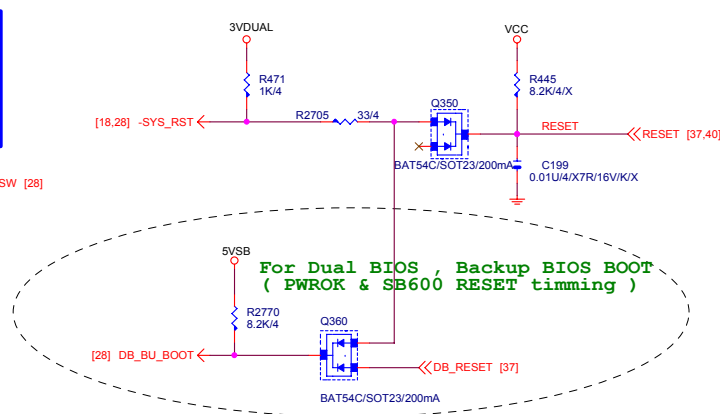
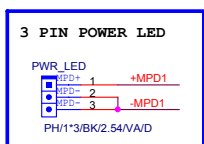
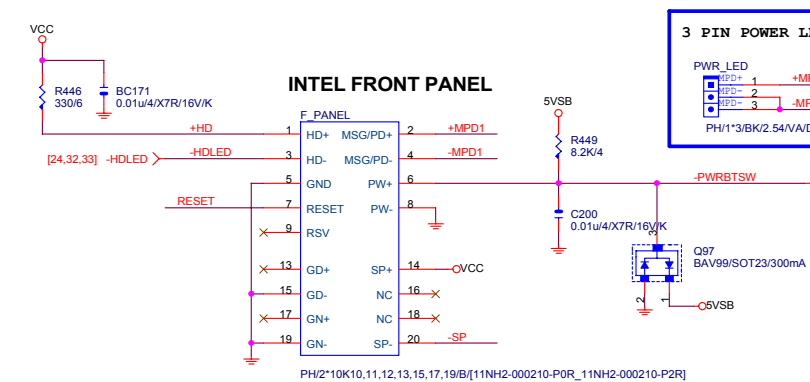
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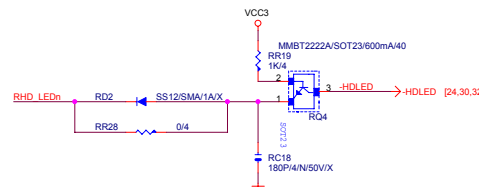
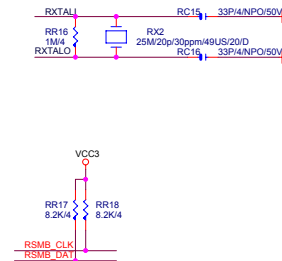
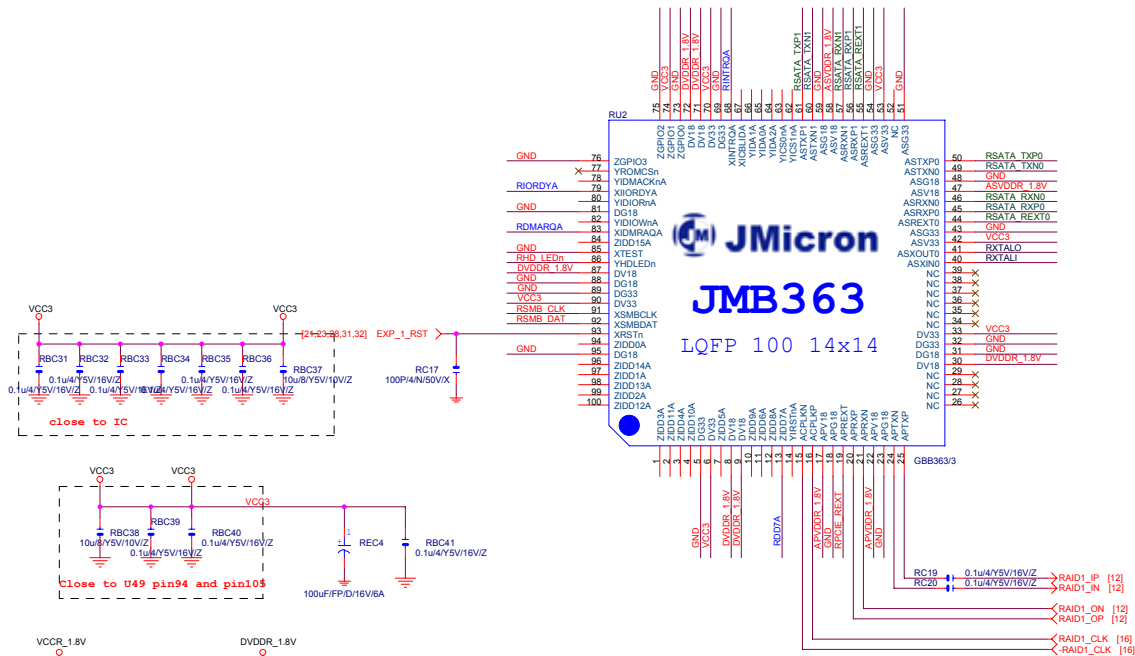
Hardware Monitor circuits



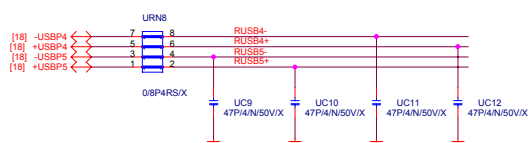
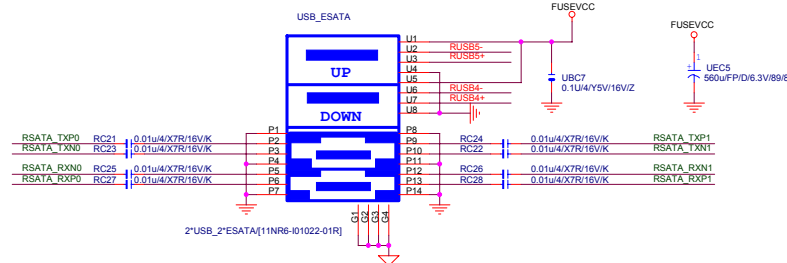
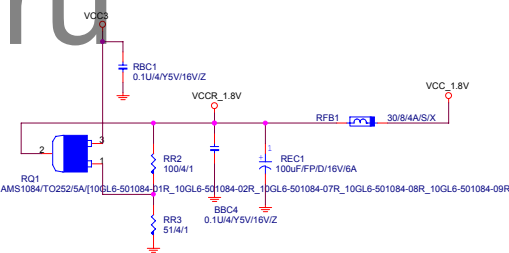
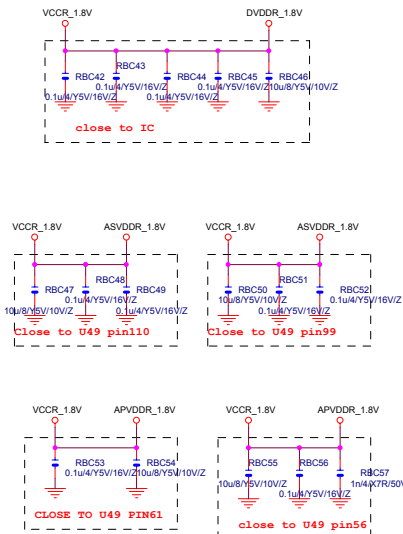
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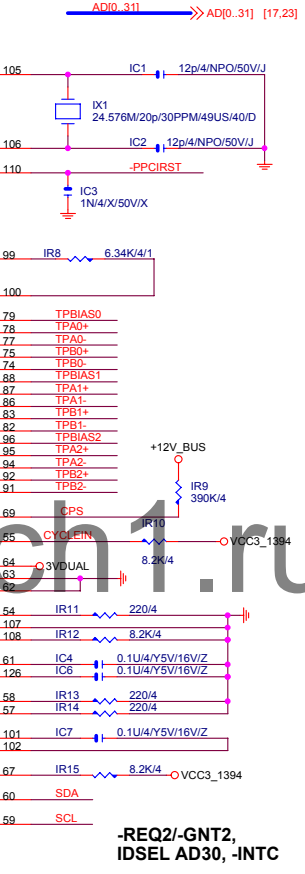
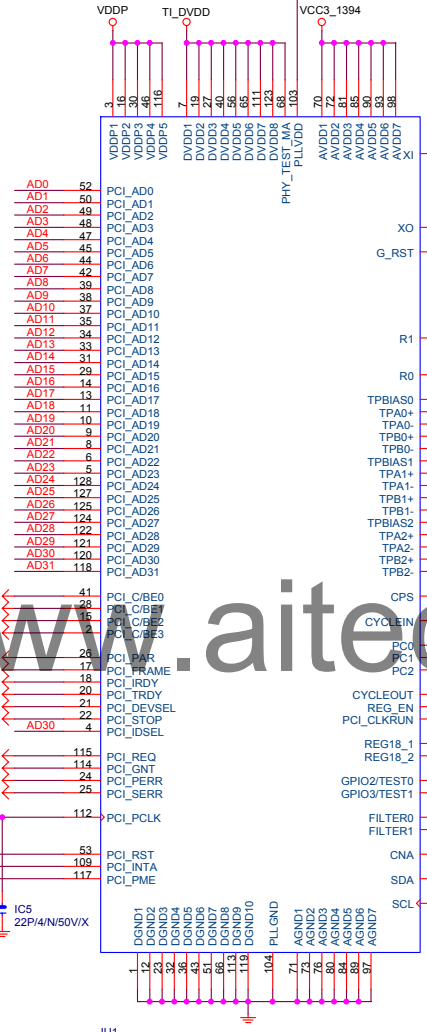
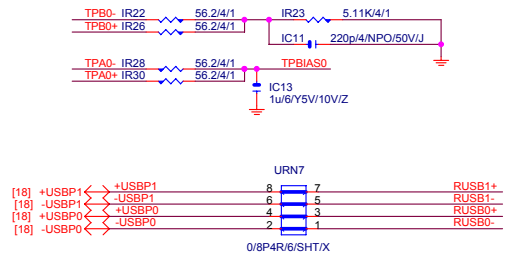
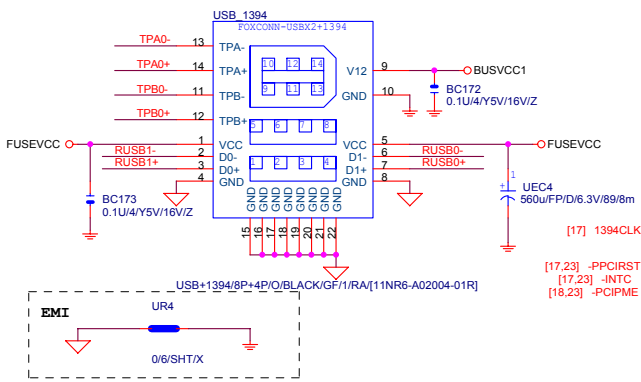
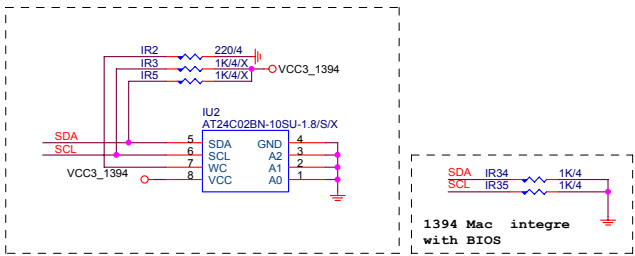
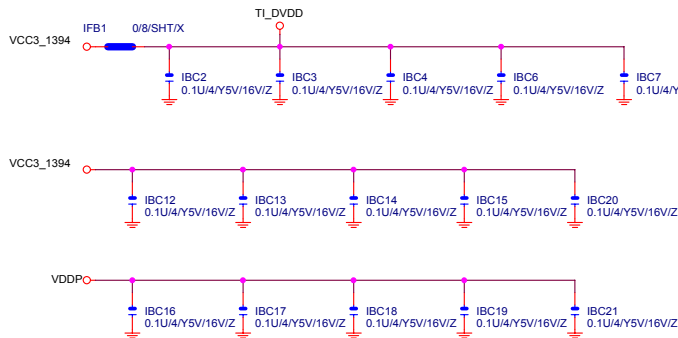
For Seasonic 900W Power supply cant Boot issue



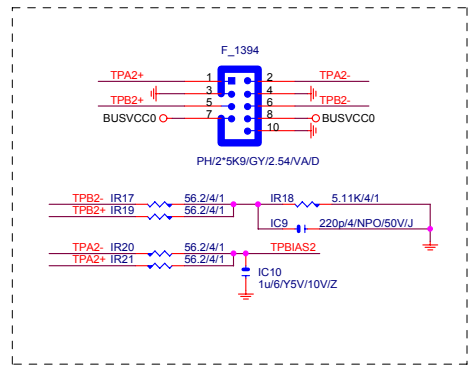
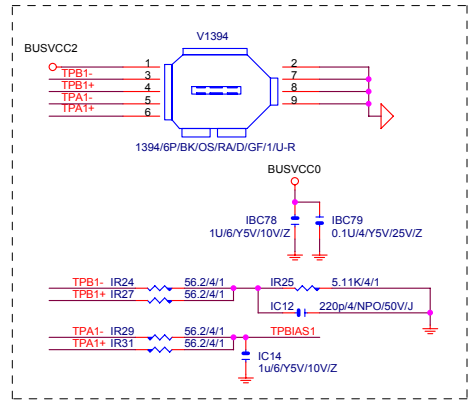
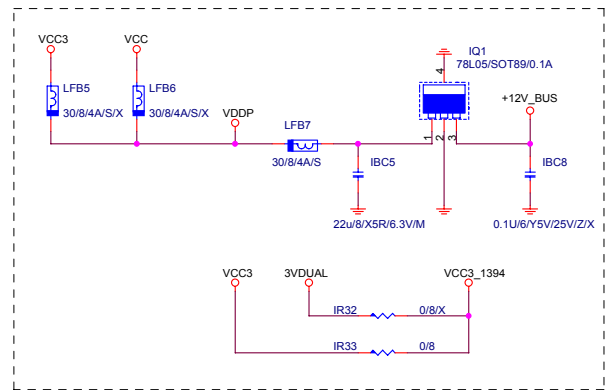
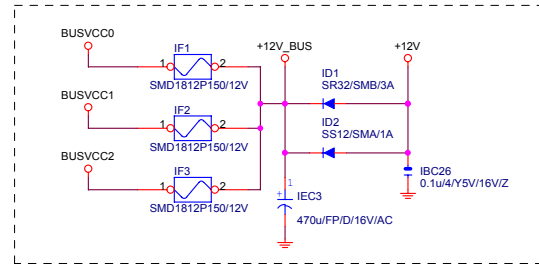
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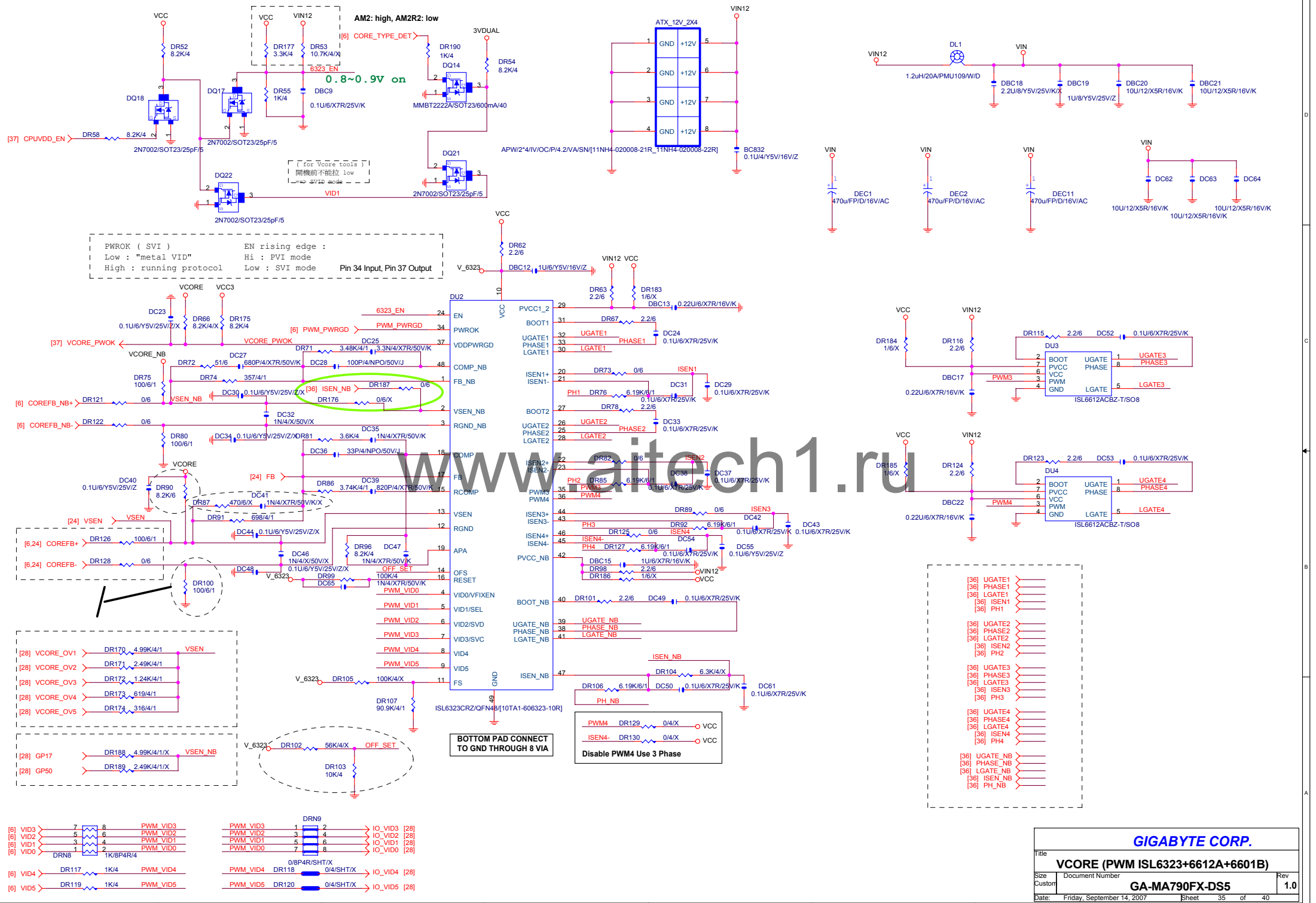


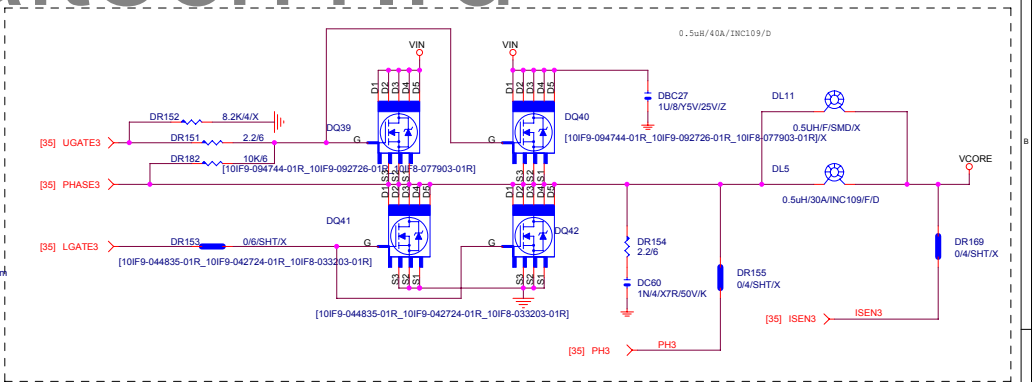
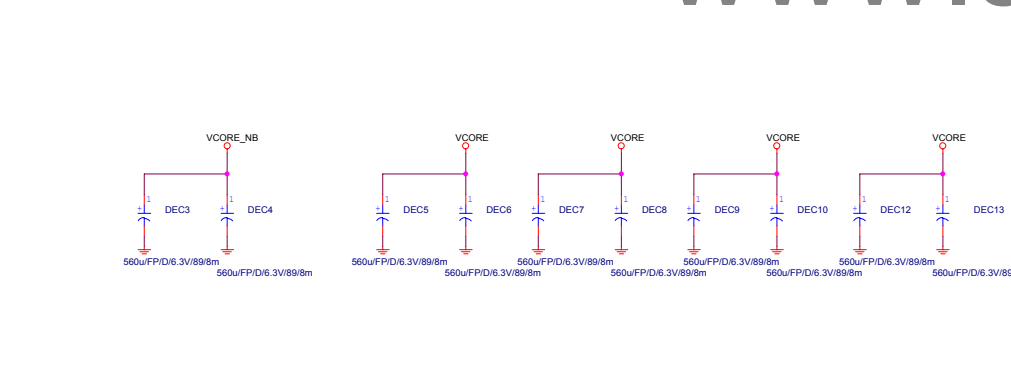
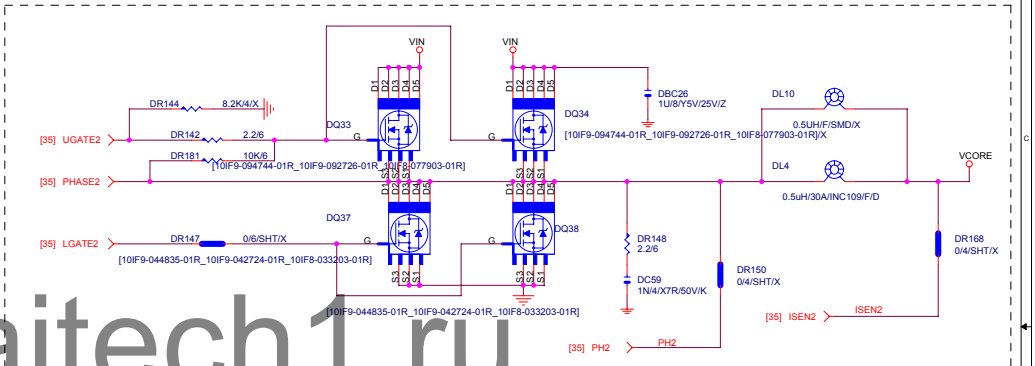
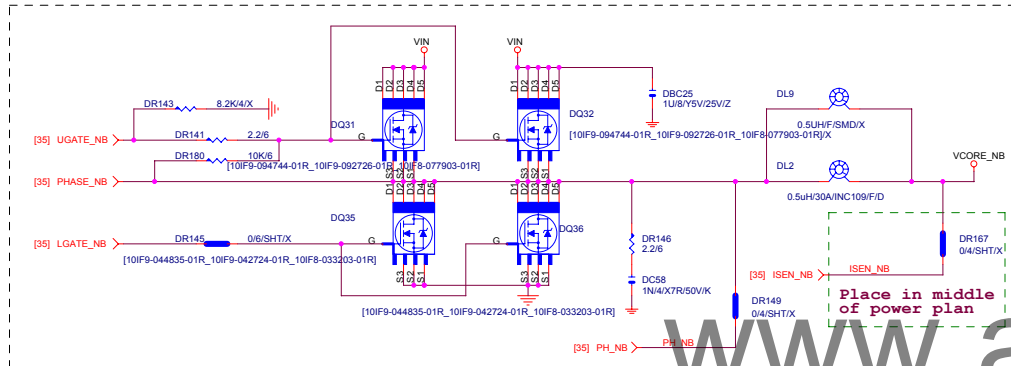
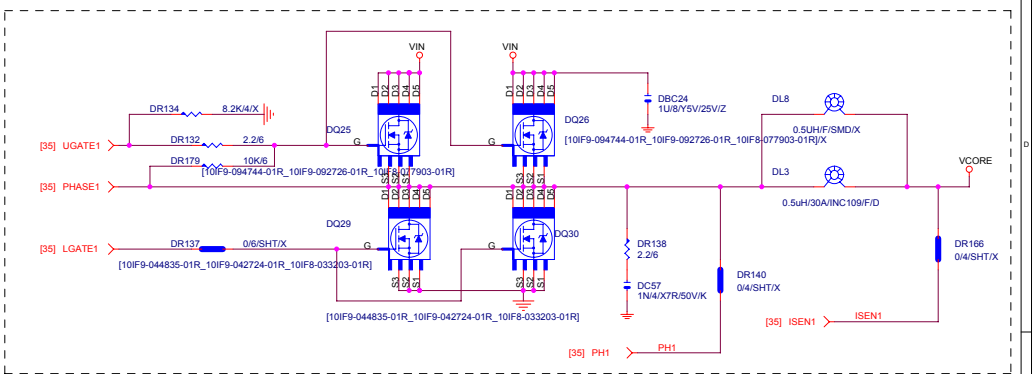
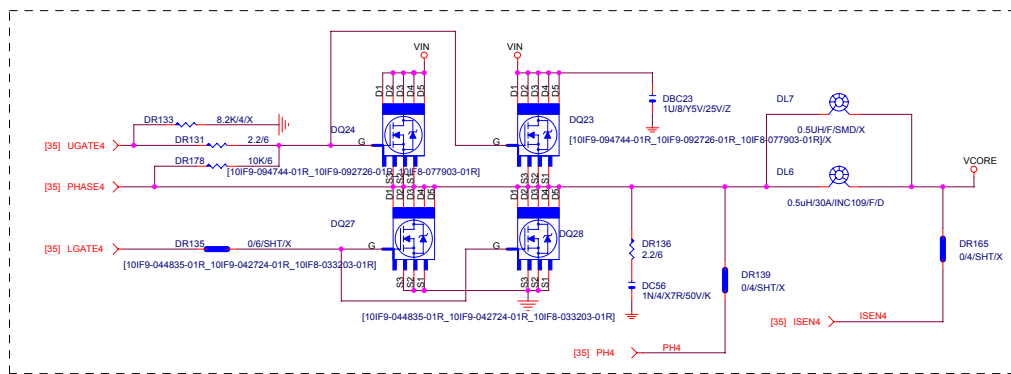
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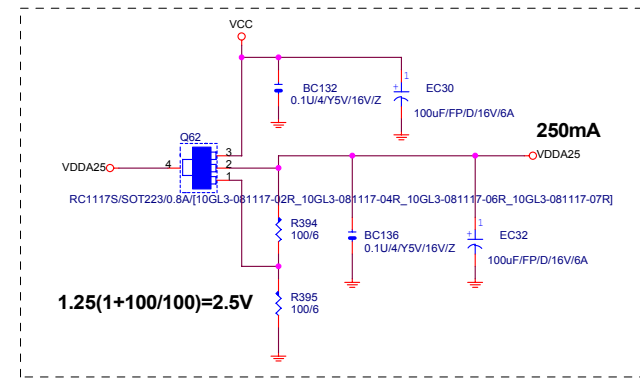
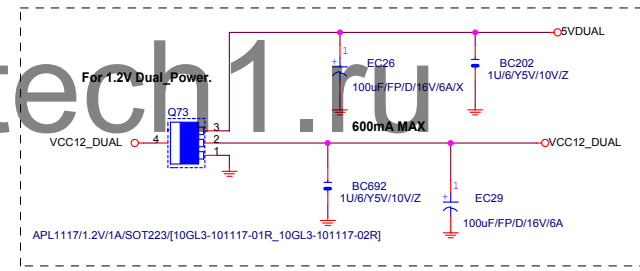
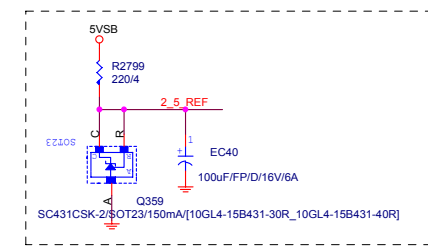
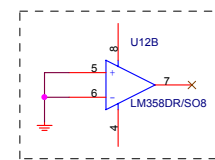
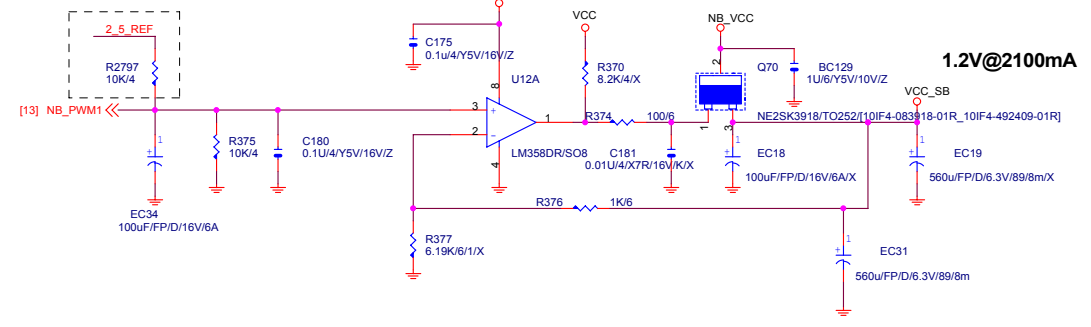
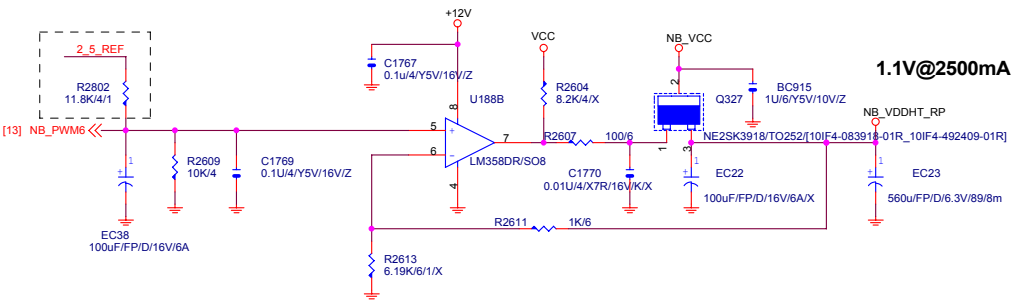
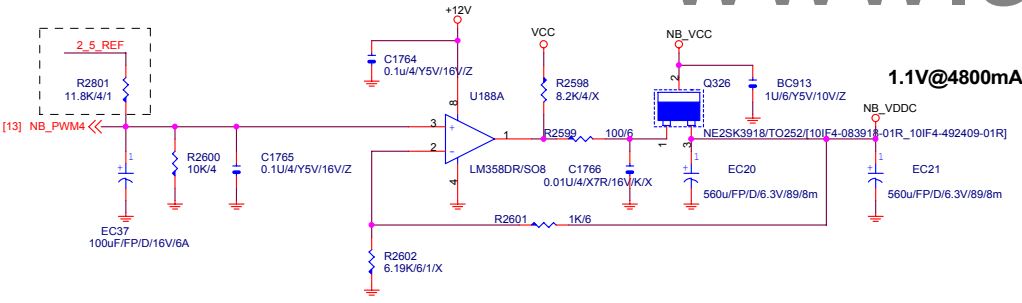
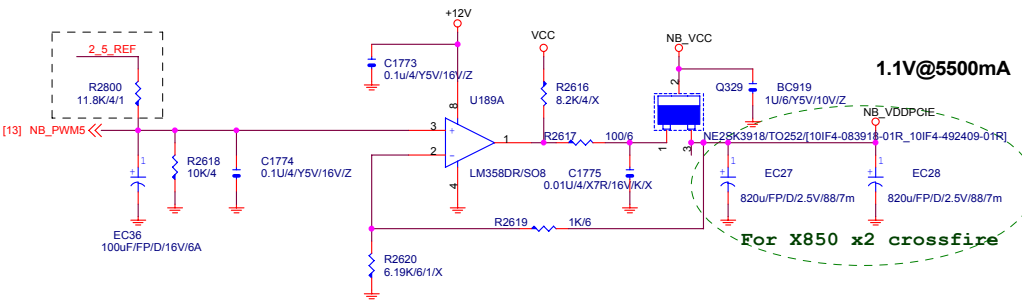
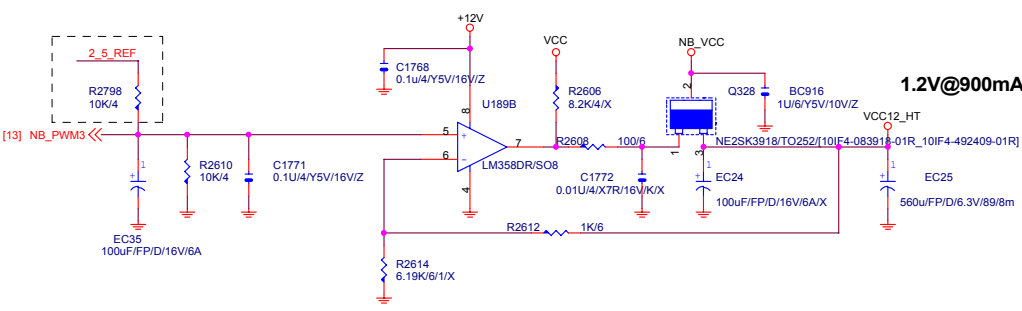


-REQ2/-GNT2,
IDSEL AD30, -INTC



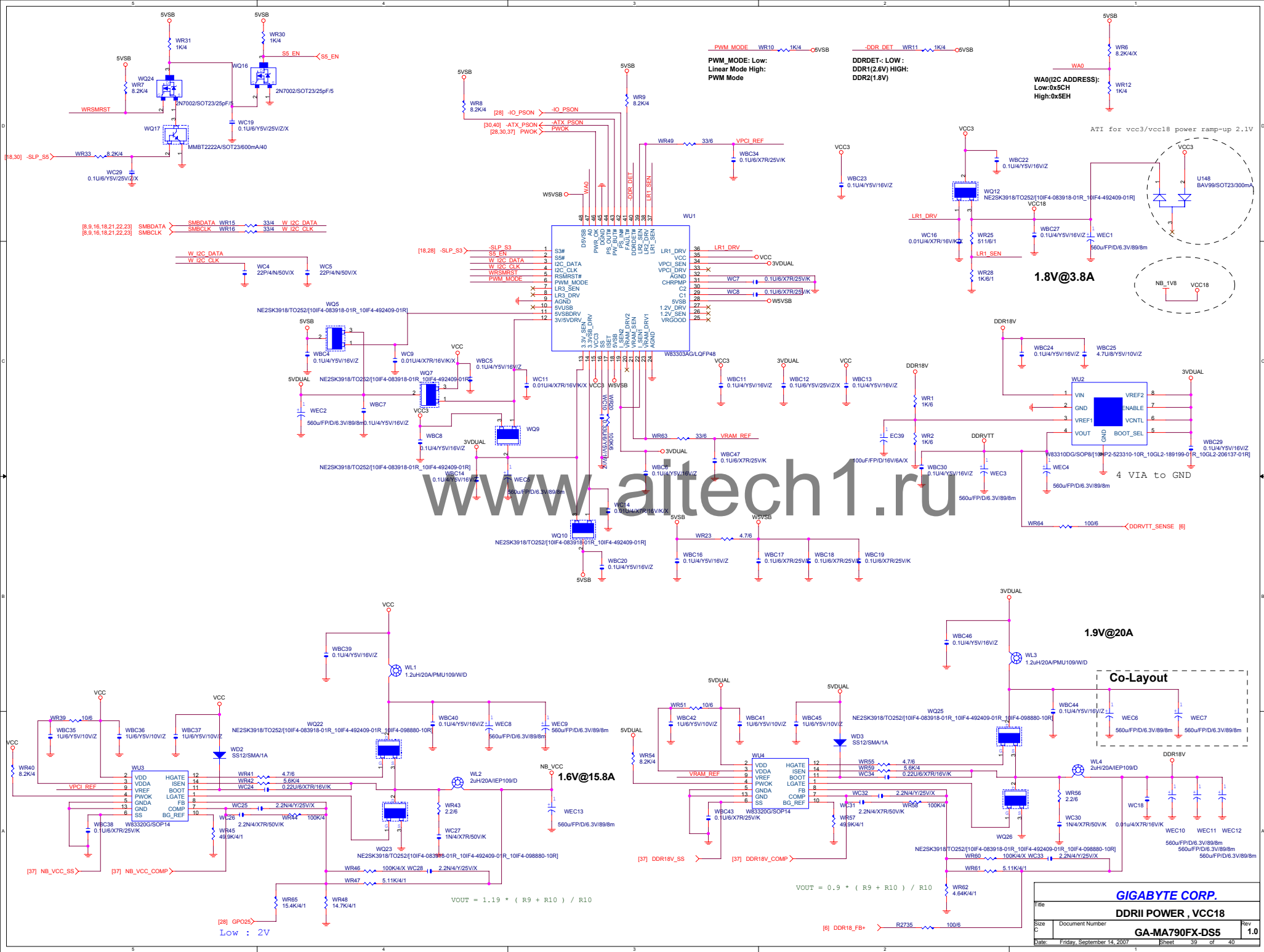


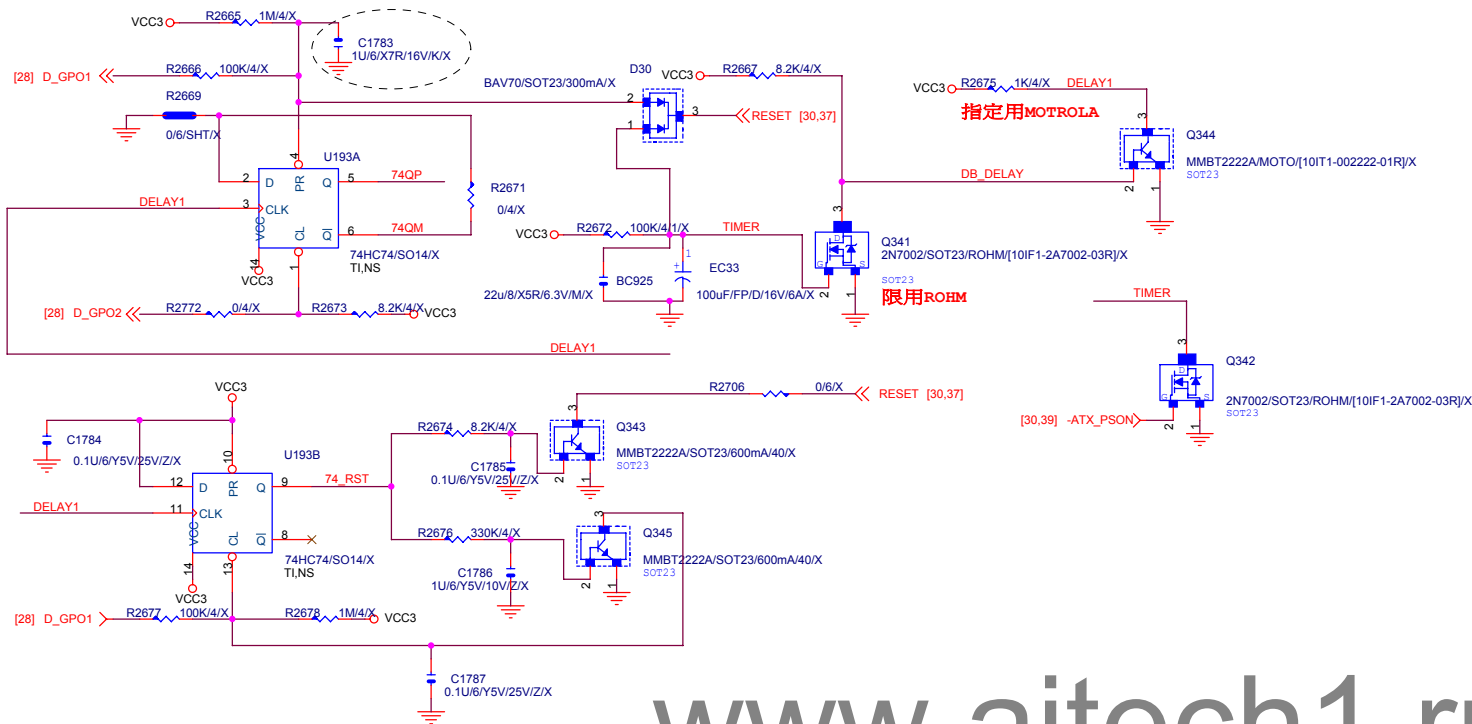




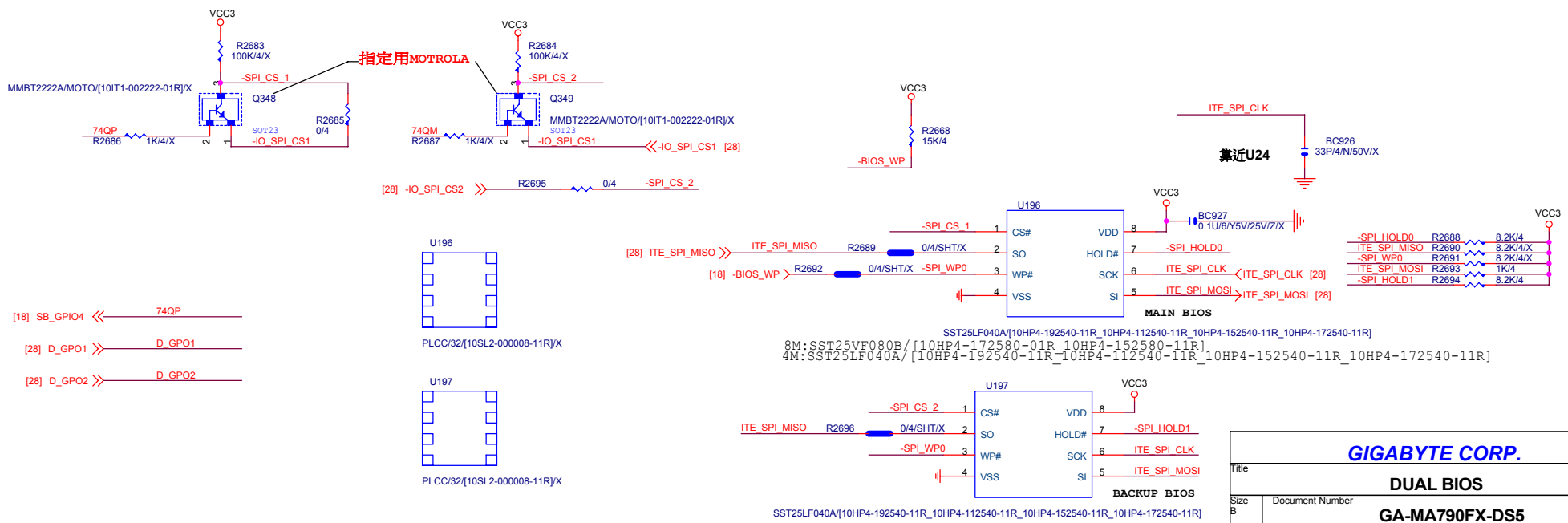
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